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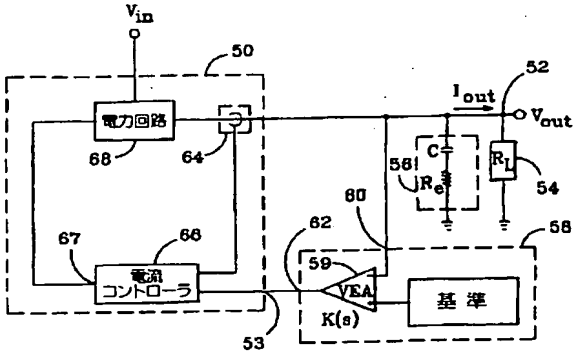
(54)【発明の名称】　電圧レギュレータの負荷過渡応答を改善し出力コンデンサ・サイズを最小化する方法および装置

(57)【要約】
【課題】　負荷電流における大きな双方向ステップ変化に対して指定された境界以内にレギュレータの出力電圧（V_{out}）を維持させる、可能な限り最小の出力コンデンサ（５６）を使用することを電圧レギュレータに可能にする方法および回路を提供する。
【解決手段】　これを達成するに当たり、負荷電流におけるステップ変化（ΔI_{load}）に対して、許容される最大値（ΔV_{out}）以下のピーク電圧偏差を確保する、可能な限り最大の等価直列抵抗（ＥＳＲ）と可能な限り低い容量との組み合わせを有する出力コンデンサを採用し、ピーク偏差の発生後平坦となる応答を確保するようにレギュレータを補償する。本発明は、スイッチングおよび線形電圧レギュレータ双方に適用可能である。



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【特許請求の範囲】

【請求項１】　負荷電流における双方向ステップ変化に対して指定された境界以内にレギュレータの出力電圧を維持させる、可能な限り最小の出力コンデンサを使用することを電圧レギュレータに可能にする方法であって、出力コンデンサ（５６）を採用し、負荷電流における双方向ステップ変化に対して指定された境界以内に規制出力電圧（V_{out}）を維持することが必要な電圧レギュレータを、その出力電圧がそのピーク偏差に達した後にその応答が平坦となるように補償するステップから成り、前記補償を行うために必要な前記出力コンデンサが、前記指定された境界以内に前記レギュレータの出力電圧を維持させる、前記可能な限り最小の出力コンデンサである、ことを特徴とする方法。

【請求項２】　負荷電流における双方向ステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に電圧レギュレータの出力電圧を維持させる、前記レギュレータの出力コンデンサのサイズを最小化する方法であって、

出力ノード（５２）において負荷（R_L）に出力電圧（ΔV_{out}）を供給する電圧レギュレータが採用する出力コンデンサ（５６）の最大等価直列抵抗$R_{e(max)}$を計算するステップであって、前記出力コンデンサを前記負荷間に並列に接続し、前記レギュレータが、負荷電流における双方向ステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に電圧レギュレータの出力電圧を維持する必要があり、$R_{e(max)}$を$R_{e(max)} = \Delta V_{out} / \Delta I_{load}$にしたがって計算するステップと、

ΔI_{load}に等しい負荷電流におけるステップ増加に対して、前記出力負荷および出力コンデンサの並列結合に向けて、前記電圧レギュレータが注入する電流の最大可用勾配の絶対値、およびΔI_{load}に等しい負荷電流におけるステップ減少に対して、前記出力負荷および出力コンデンサの並列結合に向けて注入する電流の最小可用勾配の絶対値を決定するステップと、

前記絶対値の内小さい方を判定し、該絶対値の小さい方を値mとするステップと、

$C_{crit} = \Delta I_{load} / m R_{e(max)}$にしたがって、クリティカル容量$C_{crit}$を決定するステップと、

$R_{e(max)}$より多少小さいかあるいはこれに等しい等価直列抵抗R_e、およびC_{crit}以上の容量を有する出力コンデンサを、前記負荷間に接続するために選択するステップと、

前記電圧レギュレータの出力インピーダンスをR_eにほぼ等しくなるように構成するステップと、から成ることを特徴とする方法。

【請求項３】　請求項２記載の方法において、前記電圧レギュレータが、制御入力（５３）において受け取る信号に応答して前記レギュレータの出力電圧を供給する可制御電力段（５０）と、前記出力ノードおよび前記制御

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入力間に接続された電圧誤差増幅器（５９）とを含み、前記電力段がトランスコンダクタンスgによって特徴付けられ、前記出力インピーダンスをR_eにほぼ等しくなるように調整するステップを実行する際に、前記電圧誤差増幅器の利得K（s）を、

【数１】

$K(s) = (-1/gR_e)(1/(1+sR_eC))$

に等しくし、ここで、CおよびR.は、前記採用した出力コンデンサの容量および等価直列抵抗である、ことを特徴とする方法。

【請求項４】　負荷電流における双方向ステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内にバック型スイッチング電圧レギュレータの出力電圧V_{out}を維持することを可能にする、前記レギュレータの出力コンデンサのサイズを最小化する方法であって、

入力電圧V_{in}を受け取り、出力インダクタ（L）を介して出力ノード（５２）に接続された負荷（R_L）に出力電圧（ΔV_{out}）を供給する電流制御型スイッチング電圧レギュレータが採用する出力コンデンサ（５６）の最大等価直列抵抗$R_{e(max)}$を計算するステップであって、前記インダクタを第１および第２スイッチ（７２，７４）によってV_{in}および接地に交互に接続し、前記出力コンデンサが前記負荷間に並列に接続され、前記レギュレータが、負荷電流における双方向ステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内にV_{out}を維持する必要があり、$R_{e(max)}$を

【数２】$R_{e(max)} = \Delta V_{out} / \Delta I_{load}$

にしたがって計算するステップと、

【数３】$L_{min} = V_{out} T_{off} R_{e(max)} / V_{ripple\,p\text{-}p}$

にしたがって前記出力インダクタに対する最小インダクタンスL_{min}を決定するステップであって、ここで、T_{off}は前記第１スイッチのオフ時間、$V_{ripple\,p\text{-}p}$は最大許容ピーク対ピーク出力リップル電圧である、ステップと、

前記レギュレータにおいて使用するために、L_{min}以上のインダクタンスＬ１を有する出力インダクタを選択するステップと、

$V_{out} < (V_{in} - V_{out})$の場合、

【数４】

$C_{min} = \Delta I_{load} / [R_{e(max)} (V_{out} / L1)]$

にしたがい、

$V_{out} > V_{in} - V_{out}$の場合、

【数５】$C_{min} = \Delta I_{load} / [R_{e(max)} ((V_{in} - V_{out}) / L1)]$

にしたがって、前記出力コンデンサの最小容量C_{min}を決定するステップと、

C_{min}にほぼ等しい容量Cを有する出力コンデンサ、および$R_{e(max)}$にほぼ等しい等価直列抵抗R_eを有する出力コンデンサを、前記負荷間に接続するために選択するステップと、

前記レギュレータの出力インピーダンスをR_eにほぼ等しくなるように構成するステップと、から成ることを特徴とする方法。

【請求項５】　負荷電流における双方向ステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に出力電圧を維持する電圧レギュレータであって、

トランスコンダクタンスｇによって特徴付けられ、制御入力（５３）において受け取る信号に従って出力ノード（５２）に出力電圧V_{out}を生成するように接続され、前記出力ノードが負荷（R_L）に接続されている、可制御電力段（５０）と、

前記出力ノードに接続され、および前記負荷間に並列に接続された出力コンデンサ（５６）であって、等価直列抵抗R_eを有する、出力コンデンサと、

前記出力ノードと前記制御入力との間に接続された電圧誤差増幅器（５９）とを備え、前記可制御電力段、前記出力コンデンサおよび前記増幅器が、負荷電流におけるステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に、前記出力ノードにおける電圧を維持する必要がある電圧レギュレータを形成し、

前記出力コンデンサが、クリティカル容量C_{crit}以上の容量を有し、該クリティカル容量C_{crit}を、

【数６】$C_{crit}=\Delta I_{load}/mR_e$

にしたがって決定し、ここで、ｍは、１）ΔI_{load}に等しい負荷電流におけるステップ増加に対して、前記出力負荷および出力コンデンサの並列結合に向けて、前記電圧レギュレータが注入する電流の最大可用勾配の絶対値、および２）I_{load}に等しい負荷電流におけるステップ減少に対して、前記出力負荷および出力コンデンサの並列結合に向けて、前記電圧レギュレータが注入する電流の最小可用勾配の絶対値の内小さい方に等しく、前記電圧レギュレータが、R_eにほぼ等しい出力インピーダンスを有するように構成されている、ことを特徴とする電圧レギュレータ。

【請求項６】　請求項５記載の電圧レギュレータにおいて、前記電圧誤差増幅器の利得Ｋ（ｓ）が、

【数７】

$K(s)=(-1/gR_0)(1/1+sR_eC))$

によって与えられ、ここで、ｇは前記可制御電力段のトランスコンダクタンスに等しく、R_eおよびＣは、それぞれ、前記出力コンデンサの等価直列抵抗および容量に等しい、ことを特徴とする方法。

【請求項７】　請求項５記載の電圧レギュレータにおいて、前記出力コンデンサが、C_{crit}にほぼ等しい容量、および$\Delta V_{out}/\Delta I_{load}$にほぼ等しい等価直列抵抗$R_e$を有し、前記コンデンサは、電圧レギュレータが負荷電流におけるステップ変化ΔI_{load}に対してその出力電圧をΔV_{out}以内に維持することを可能にする、可能な限り最小の出力コンデンサであることを特徴とする電圧レギュレータ。

【請求項８】　負荷電流におけるステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に規制出力電圧を維持する電圧レギュレータであって、

第１制御入力（１０２）および第２制御入力（１０４）間の電圧差に応じて、出力ノード（５２）において負荷（R_L）に出力電圧（V_{out}）を供給する可制御電力段（１００）と、

前記出力ノード、および前記負荷間に並列に接続された出力コンデンサ（５６）と、

前記出力ノードおよび第１ノード（１１０）間に接続されたインピーダンスＺ１と、

前記第１ノードおよび基準電圧（V_{ref}）間に接続されたインピーダンスＺ２と、

トランスレジスタンスR_sを有し、前記負荷に送出される出力電流（I_{out}）と共に変動する出力電圧（V_{out}）を生成する電流センサ（１０６）と、

前記センサ出力電圧と前記出力ノードにおける電圧との和に等しい出力電圧を生成する加算回路（１０８）とを備え、前記電流センサ出力電圧および前記加算回路出力電圧が、それぞれ、前記第１および第２制御入力に接続され、前記可制御電力段、前記出力コンデンサ、前記インピーダンス、前記電流センサ、および前記加算回路が、負荷電流におけるステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に、前記出力ノードにおける電圧を維持する必要がある電圧レギュレータを形成し、前記レギュレータが、インピーダンスＺ１およびＺ２の比が、

【数８】

$Z1/Z2=[(R_0(1+sR_eC)-R_s]/R_s$

に等しくなるように構成され、ここで、R_eおよびＣは、それぞれ、前記出力コンデンサの等価直列抵抗および容量に等しく、R_0は、Ｃが$\Delta I_{load}/mR_e$以上の場合、R_eに等しく、あるいは、

Ｃが$\Delta I_{load}/mR_e$未満の場合、$\Delta I_{load}/2mC+[mC(R_e)]/2\Delta I_{load}$に等しく、

ｍは、１）ΔI_{load}に等しい負荷電流におけるステップ増加に対して、前記出力負荷および出力コンデンサの並列結合に向けて、前記電圧レギュレータが注入する電流の最大可用勾配の絶対値、および２）ΔI_{load}に等しい負荷電流におけるステップ減少に対して、前記出力負荷および出力コンデンサの並列結合に向けて、前記電圧レギュレータが注入する電流の最小可用勾配の絶対値の内小さい方に等しい、ことを特徴とする電圧レギュレータ。

【請求項９】請求項８記載の電圧レギュレータにおいて、前記インピーダンスＺ１が、並列に接続された抵抗器Ｒ１およびコンデンサＣ１によって実現され、インピーダンスＺ２が抵抗Ｒ２によって実現され、前記抵抗Ｒ１およびＲ２ならびにコンデンサC_1が、前記電圧レギュレータの出力インピーダンスがR_eに等しくなるよう

に構成され、これによって、

【数９】Ｒ２／Ｒ１＝（R_o－R_s）／R_s

および

【数１０】Ｃ１＊Ｒ１＝Ｃ［（$R_o$$R_*$）／$R_s$］

であることを特徴とする電圧レギュレータ。

【請求項１０】請求項８記載の電圧レギュレータにおいて、前記電流センサおよび加算回路が、第２ノードにおける前記可制御出力段と前記出力ノードとの間に接続された抵抗R_sを有する抵抗器を備え、前記第２ノードにおける電圧が前記加算回路の出力電圧であることを特徴とする電圧レギュレータ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、電圧レギュレータの分野に関し、更に特定すれば負荷の過渡状態に対する電圧レギュレータの応答を改善する方法に関するものである。

【０００２】

【従来の技術】電圧レギュレータの目的は、未調整の入力電圧が給電され、変動する負荷電流の要求を満たさなければならない場合であっても、負荷にほぼ一定の出力電圧を供給することである。

【０００３】用途によっては、負荷電流のステップ状変化、即ち、負荷によって要求される負荷電流の突然の大幅な増大または減少に対して、ほぼ一定の出力電圧を維持するためにレギュレータが必要となる。例えば、マイクロプロセッサが「電力節約モード」を有する場合があり、この場合使用されていない回路部分をオフにして電流消費をほぼゼロに低下させ、必要とされる場合にこれらの部分をオンとし、その際通常数百ナノ秒以内で負荷電流を高い値に上昇させなければならない。

【０００４】負荷電流に変化があると、レギュレータの出力電圧に何らかの偏差が生ずることは実際上不可避である。この偏差の大きさは、出力コンデンサの容量および等価直列抵抗（ＥＳＲ）双方に関係する。即ち、容量が小さい程またはＥＳＲが大きい程、偏差は大きくなる。例えば、スイッチング電圧レギュレータ（出力インダクタを介して出力電流を送出し、負荷間に並列に接続された出力コンデンサを含む）では、負荷電流の変化（ΔI_{load}）は、１）負荷に送出される電流が瞬時的にI_{load}だけ増大する、または２）出力コンデンサの容量が非常に大きく、更にそのＥＳＲが非常に小さいため出力電圧の偏差が無視し得る程度であるのでなければ、レギュレータの出力電圧が変化する結果となる。最初の選択肢は不可能である。何故なら、出力インダクタ内の電流は瞬時に変化することができないからである。負荷電流の変化に対処するために必要な時間は、出力インダクタのインダクタンスを小さくすることによって短縮することができるが、このためには結局レギュレータのスイッチング周波数の上昇が必要となり、スイッチング・トランジスタの有限なスイッチング速度およびトランジスタの駆動回路における消散によって制限される。２番目の選択肢は可能であるが、非常に大きな出力コンデンサが必要となり、プリント回路ボード上に占める空間が余りに大きすぎるか、コストがかかり過ぎるか、あるいはこの双方となる可能性が高い。

【０００５】レギュレータの出力電圧を、狭い負荷過渡応答仕様、即ち、負荷電流の双方向のステップ変化に対して許容可能な出力電圧の偏差を狭く制限する仕様を満たさなければならない用途では、この不可避な偏差が容認できない程大きくなる可能性がある。ここで用いる場合、「ΔV_{out}」は、レギュレータの出力電圧偏差仕様を意味すると共に、グラフに示すピーク対ピーク出力電圧偏差を意味するものとする。負荷過渡応答を改善するための最も明白な解決策は、出力容量の増大および／または出力コンデンサのＥＳＲの減少である。しかしながら、先に記したように、出力コンデンサが大きくなる程（容量が大きくなり、ＥＳＲが小さくなる）、必要な体積（ｖｏｌｕｍｅ）が大きくなり、ＰＣボード面積を広くしなければならないため、コスト上昇を招く。

【０００６】負荷過渡応答を改善する手法の１つを、図１に示す。スイッチング電圧レギュレータ１０は、電源電圧V_{in}と接地との間に接続されたプッシュ・プル・スイッチ１２を含む。これは、通常、２つの同期的に切り替えられるパワーＭＯＳＦＥＴ１４および１６によって実現する。ドライバ回路１８が接続され、ＭＯＳＦＥＴ１４および１６の一方または他方を交互に切り替える。デューティ比変調回路２０が駆動回路を制御する。回路２０は、クロック回路２４から受ける鋸波クロック信号および誤差信号発生回路２６から受ける誤差電圧を比較する電圧比較器２２を含む。通常、回路２６は、高利得演算増幅器２８を含み、一方の入力において基準電圧V_{ref}、および第２入力において出力電圧V_{out}の電圧表現を受け、V_{out}と所望の出力電圧との差と共に変動する誤差電圧を生成する。また、レギュレータは、ＭＯＳＦＥＴ１４および１６の間の接合点に接続された出力インダクタＬ、等価直列抵抗R_*と直列な容量Ｃとして表現して示されている出力コンデンサ３０、ならびに出力インダクタおよび出力コンデンサ間に接続された抵抗器R_sも含む。V_{out}が接続され、負荷３２を駆動する。

【０００７】動作において、ＭＯＳＦＥＴ１４および１６は、インダクタＬをV_{in}および接地に交互に接続するように駆動され、デューティ比は、デューティ比変調回路２０によって決定される。デューティ比は、誤差増幅器２８が生成する誤差電圧に応じて変動する。インダクタＬの電流は、出力コンデンサ３０および負荷３２の並列結合に流れ込む。コンデンサ３０のインピーダンスは、スイッチング周波数では、負荷３２のそれよりも遥かに小さいので、コンデンサはインダクタ電流のＡＣ成分の殆どを濾過して除去し、事実上直流の全てが負荷３

２に送出される。

【０００８】直列抵抗器R_sがないと、回路２６にフィードバックされる電圧はV_{out}に等しくなり、レギュレータの負荷電流におけるステップ変化に対する応答は、典型的なスイッチング・レギュレータのそれとなる。図２ｂに示す負荷電流I_{load}のステップ変化に対するレギュレータの出力電圧V_{out}を図２ａに示す。Ｌの電流は瞬時に変化することができないので、I_{load}が突然変化すると、V_{out}がスパイク状に低下し、最終的に制御ループがV_{out}を公称出力電圧V_{nom}に引き戻す。同様に、I_{load}がその後ステップ状に低下した場合、V_{out}はスパイク状に上昇し、その後V_{nom}に戻る。負荷電流のステップ変化に対する出力電圧ΔV_{out}における全偏差は、２つの電圧スパイクのピーク間の差によって決定される。レギュレータが狭い負荷過渡応答仕様に拘束されている場合、この偏差は許される許容範囲を超過する可能性がある。

【０００９】抵抗R_sをインダクタＬと直列に接続することによって（出力端子３４において）、ΔV_{out}を減少させることができる。図３ｂに示す負荷電流のステップ変化に対して、R_sを含む場合に可能な応答の１つを図３ａに示す。R_sが適所に含まれる場合、制御ループはもはやV_{out}をV_{nom}に復元させるのではなく、むしろV_{out}は、端子３４における電圧からΔI_{load}およびR_sの積を減じた値によって与えられる電圧に復元する。即ち、軽い負荷に対するV_{out}の定常状態値は、重い負荷に対する場合よりも、$\Delta_{load} * R_s$だけ高くなる。R_sを出力コンデンサのＥＳＲにほぼ等しくすることによって、R_sを使用しない場合に得られるよりも、いくらか狭いΔV_{out}を得ることができる。

【００１０】図１の回路の欠点について、その１つを図４ａおよび図４ｂに示す。この場合、負荷電流（図４ｂ）は、V_{out}（図４ａ）が定常状態値に静定する前に、再びステップ状に低下する。I_{load}が低下する時点においてV_{out}が図３ａにおけるよりも高いと、上向きのV_{out}スパイクのピークも高くなり、全体的な偏差ΔV_{out}は、それ以外の場合よりも大きくなる。このように偏差が大きくなるのは、特に狭い出力電圧偏差仕様を満たすためには、レギュレータ１０はより大きな出力コンデンサを使用しなければならず、そのＥＳＲは比例的に小さくなることを意味する。コンデンサのコストは、近似的にそのＥＳＲに反比例するので、この仕様を満たすのは過度に費用がかかる可能性がある。

【００１１】図１の回路の別の欠点は、直列抵抗器ＲＳにかなりの電力消費が必要となることである。例えば、R_sを５ｍΩ、最大負荷電流を１４．６Ａと仮定すると、R_sにおける消費は１．０７Ｗとなる。

【００１２】レギュレータの負荷過渡応答を改善するに当たり、異なる制御原理を用いた手法が、Ｄ．Ｇｏｄｅｒ（Ｄ．ゴーダ）およびＷ．Ｒ．Ｐｅｌｌｅｔｉｅｒ（Ｗ．Ｒ．ペレチア）の“V^2 Ａｒｃｈｉｔｅｃｔｕｒｅ Ｐｒｏｖｉｄｅｓ Ｕｌｔｒａ?Ｆａｓｔ Ｔｒａｎｓｉｅｎｔ Ｒｅｓｐｏｎｓｅ ｉｎ Ｓｗｉｔｃｈ Ｍｏｄｅ Ｐｏｗｅｒ Ｓｕｐｐｌｉｅｓ”（V^2アーキテクチャはスイッチ・モード電源において超高速過渡応答をもたらす）、ＨＦＰＣ ＰｏｗｅｒＣｏｎｖｅｒｓｉｏｎ、１９９６年９月、Ｐｒｏｃｅｅｄｉｎｇｓ、１９－２３ページに開示されている。この中に記載されているレギュレータは、プッシュ・プル・スイッチ、ドライバ回路、誤差増幅器、ならびに図１に示したのと同様の出力インダクタおよびコンデンサを含む。レギュレータの出力電圧を表わす信号が、誤差増幅器および電圧比較器双方に供給される。電圧比較器は、誤差増幅器の出力も受け取る。レギュレータの出力電圧が誤差増幅器の出力を超過した場合、比較器の出力は高に移行し、単安定マルチバイブレータをトリガし、所定の時間間隔にわたって上側のスイッチング・トランジスタをオフにする。

【００１３】この回路の過渡応答は、図１の回路のそれよりも高速となるように設計されている。負荷電流のステップは、比較器における電圧を直ちに変化させ、鈍い誤差増幅器を迂回し、これによって応答時間を短縮する。しかしながら、応答時間が短くなっても、応答トレースの形状は依然として図３ａに示すものと類似しており、ΔV_{out}の大きさには殆どなんの改善もない。

【００１４】別のスイッチング・レギュレータが、Ｌ．Ｓｐａｚｉａｎｉ（Ｌ．スパッチアーニ）の“Ｆｕｅｌｉｎｇ ｔｈｅ Ｍｅｇａｐｒｏｃｅｓｓｏｒ ? ａ ＤＣ／ＤＣ Ｃｏｎｖｅｒｔｅｒ Ｄｅｓｉｇｎ Ｒｅｖｉｅｗ Ｆｅａｔｕｒｉｎｇ ｔｈｅ ＵＣ３８８６ ａｎｄ ＵＣ３９１０”（メガプロセッサの給電？ＵＣ３８８６およびＵＣ３９１０を特徴とするＤＣ／ＤＣ変換器設計の検討）、Ｕｎｉｔｒｏｄｅ Ａｐｐｌｉｃａｔｉｏｎ Ｎｏｔｅ Ｕ?１５７、３?５４１ないし３?５７０ページに記載されている。このレギュレータは、出力インダクタにおける電流の平均値を制御することによって調整を行う、「平均電流制御」として知られている制御原理を採用している。レギュレータの出力インダクタと直列に抵抗器を接続し、この抵抗器間に電流検知増幅器（ＣＳＥ：ｃｕｒｒｅｎｔ ｓｅｎｓｅ ａｍｐｌｉｆｉｅｒ）を接続してインダクタ電流を検知する。ＣＳＥの出力は、電圧誤差増幅器の出力と共に、電流誤差増幅器に供給される。電圧誤差増幅器は、レギュレータの出力電圧を基準電圧と比較する。比較器は、一方の入力において電流誤差増幅器の出力、他方の入力において鋸波クロック信号を受け取る。比較器は、パルス幅変調出力を生成し、ドライバ回路を介してプッシュ・プル・スイッチを駆動する。

【００１５】動作において、負荷電流の増大により、出力電圧が減少し、電圧誤差増幅器からの誤差信号が増大

する。このために、電流誤差増幅器からの出力が増大し、そのため比較器が生成するパルスのデューティ比が大きくなる。すると、出力インダクタ内の電流が増大し、出力電圧を押し上げる。電圧誤差増幅器は、非積分利得を与えるように構成されており、これが、平均電流制御との組み合わせで、レギュレータに、有限で制御可能な出力抵抗を与える。これにより、出力電圧の位置付けは、直列抵抗器R_sが図１の回路の応答に影響を与える態様と同様となる。しかしながら、参考文献の図３２に明確に示されているように、得られる応答はこの場合も図３ａのそれに類似しており、依然としてΔV_{out}が狭い出力電圧偏差仕様を超過する可能性がある。

【００１６】

【発明が解決しようとする課題】先に記した問題を克服し、可能なかぎり最少の出力コンデンサを使用しつつ電圧レギュレータが大きな双方向負荷過渡状態に対して最適な応答を得ることができる方法および回路を提供する。

【００１７】

【課題を解決するための手段】本発明は、出力コンデンサのサイズおよびコストを最小に抑えることが好ましく、その出力電圧を、負荷電流の大きな双方向ステップ変化に対して指定された境界以内に維持しなければならない電圧レギュレータと共に用いることを意図するものである。これらの目標を達成するに当たり、負荷電流における双方向ステップ変化に対するピーク対ピーク電圧偏差が許容最大値以下であることを補償する、可能な限り最大の等価直列抵抗（ＥＳＲ）と可能な限り最低の容量との組み合わせを有する出力コンデンサを採用し、ここでは「最低応答」と呼ぶ、ピーク偏差の発生後に平坦となる応答を確保するように、レギュレータを補償する。これらの条件を満たすと、レギュレータの出力コンデンサは、負荷電流における双方向ステップ変化に対して指定された境界以内に、出力電圧を留まらせることを可能にする、可能な限り最小のコンデンサとなる。本発明は、スイッチングおよび線形電圧レギュレータ双方に適用可能である。

【００１８】本発明の更に別の特徴および利点は、添付図面と共に以下の詳細な説明を参照することにより、当業者には明白となろう。

【００１９】

【発明の実施の形態】本発明は、負荷電流に大きな双方向ステップ状変化を必要とする用途において、電圧レギュレータの出力に使用可能な、可能な限り最小のコンデンサを決定する手段を提供する。これにより、レギュレータの出力電圧は、所与のステップ・サイズに対して指定される境界以内に維持することが可能となる。ここでは、負荷電流における所与のステップ変化をΔI_{load}として識別し、許容可能な出力電圧偏差仕様をΔV_{out}として識別する。ここで用いる場合、「可能な限り最小の出力コンデンサ」とは、レギュレータがΔV_{out}仕様を満たすことを可能にする、可能な限り最小の容量値および許され得る最大のＥＳＲ値を有する出力コンデンサのことを意味するものとする。コンデンサのコストは、そのＥＳＲに反比例し、その容量に直接比例する傾向があるので、そして空間は殆ど常に回路ボード上では貴重であるので、本発明は、出力コンデンサのコストおよび空間要件を最小化することを可能にするものである。

【００２０】本発明は、適正に構成された電圧レギュレータを用いれば、レギュレータが所与のΔV_{out}仕様を満たすことを可能にする、可能な限り最小の出力コンデンサがあるという現実を利用するものである。出力コンデンサの等価直列インダクタンスの効果を無視すると、負荷電流のステップ変化ΔI_{load}は、電圧レギュレータの出力電圧に初期変化を発生させる。これは、コンデンサのＥＳＲ（ここではR_eとして識別する）およびΔI_{load}の積、即ち、$R_e * \Delta I_{load}$に等しい。この初期変化は、上方向および下方向双方の負荷電流ステップに生じる。出力コンデンサの容量Ｃがある「クリティカル（ｃｒｉｔｉｃａｌ）」値C_{crit}（以下で詳しく論ずる）以上である場合、出力電圧偏差は初期の$R_e * \Delta I_{load}$変化を超過することができない。ＣがC_{crit}未満である場合、出力電圧偏差は、初期の$R_e * \Delta I_{load}$が変化した後その後復元し始める前に増加し続ける。

【００２１】従来技術のレギュレータは、通常、負荷の過渡状態発生後に、出力電圧を公称値に向かって再度駆動するように設計されている。しかしながら、このようにすると、全体的な出力電圧偏差ΔV_{out}が、$R_e * \Delta I_{load}$の２倍にまで達する可能性がある。負荷電流がステップ状に上昇すると、V_{out}は公称電圧から$R_e * \Delta I_{load}$だけ低下する。負荷電流が十分長く高に留まっている場合、レギュレータはV_{out}を再度公称電圧に駆動する。ここで、負荷電流が再度ステップ状に低下すると、V_{out}は$R_e * \Delta I_{load}$だけスパイク状に上昇し、その結果全出力電圧偏差は２（$R_e * \Delta I_{load}$）となる。

【００２２】従来技術のレギュレータのΔV_{out}の大きさに対する制御方法に内在する欠点を認識してわかったのは、最適負荷過渡応答？即ち、最小の出力電圧偏差ΔV_{out}を生成する応答は、下向きの負荷電流ステップの後上側の電圧偏差境界にて一定に留まり、上向きの負荷電流ステップの後下側の電圧偏差境界にて一定に留まる応答であるということであった。本発明は、レギュレータの負荷過渡応答がこの理論的最適値またはその近傍となるようにレギュレータを構成する方法を提供する。また、この応答を達成するために必要な出力コンデンサは、ΔV_{out}の仕様を満たすために用いることができる、可能な限り最小のコンデンサであることがわかった。

【００２３】最適な応答を得るという目標を達成し、これによって、満たすべき所与のΔV_{out}仕様を可能にす

る可能な限り最小のコンデンサを特定するためには、多数のステップを実行しなければならない。最初に、負荷電流の双方向ステップ変化ΔI_{load}に対して指定された電圧偏差指定ΔV_{out}の制約を受ける電圧レギュレータが採用する出力コンデンサに対し、最大等価直列抵抗$R_{e(max)}$を決定する。オームの法則によれば、$R_{e(max)}$は、$R_{e(max)}=\Delta V_{out}/\Delta I_{load}$で与えられる。出力コンデンサの$R_e$が$R_{e(max)}$よりも少しでも大きい場合、$\Delta I_{load}$に等しい負荷電流のステップ変化に対する$V_{out}$の初期偏差は、必ず$\Delta V_{out}$を超過する。

【００２４】次のステップは、前述の「クリティカル」容量値C_{crit}を決定することである。クリティカル容量とは、電圧レギュレータによって駆動される負荷間に並列に（レギュレータの出力コンデンサとして）接続した＊ときに、負荷および出力コンデンサの並列結合に向かってレギュレータによって注入される電流が、レギュレータの物理的制限によって許される最大の勾配で傾斜状に上昇（または下降）する際に、出力電圧の勾配をゼロにする、即ち、初期の$R_e*\Delta I_{load}$変化後に平坦にさせる容量の量のことである。レギュレータの物理的制限によって許される最大の勾配のことを、ここでは「最大可用勾配（ｍａｘｉｍｕｍ　ａｖａｉｌａｂｌｅ　ｓｌｏｐｅ）」と呼ぶことにする。

【００２５】クリティカル容量C_{crit}は次の式で与えられる。

【００２６】

【数１１】

$$C_{crit}=\Delta I_{load}/mR_{e(max)} \quad (式2)$$

ここで、ΔI_{load}は最大予想負荷電流ステップ、$R_{e(max)}$は最大許容出力コンデンサＥＳＲ（先に計算した）、そしてｍは出力コンデンサおよび出力負荷の並列結合に向けて注入された電流に関連する勾配値であり、ｍおよびその値を決定する方法については以下で論ずる。

【００２７】傾斜パラメータｍを図５ａないし図５ｃに示す。図５ａは、上方向ステップに対する負荷電流波形を示す。図５ｂは、レギュレータが最大可用勾配ｍにおいて出力電流を生成したときの出力容量および出力負荷の並列結合に向けてレギュレータが注入した電流を示す。図５ｃは、出力コンデンサにおける電流を示し、この電流は負荷電流と注入電流との差に等しい。

【００２８】図５ｄおよび図５ｅは、レギュレータのの容量がC_{crit}よりも大きいとき（図５ｄ）およびC_{crit}よりも小さいとき（図５ｅ）に、レギュレータの出力コンデンサのサイズが、どのようにV_{out}に影響を与え、レギュレータはコンデンサおよび負荷の並列結合に向けて最大可用勾配で電流を注入するのかについて示す。$C>C_{crit}$の場合、V_{out}は、初期$\Delta I_{load}R_e$変化の発生直後に復元し始める。しかしながら、$C<C_{crit}$の場合、出力電圧の偏差は、初期$\Delta I_{load}R_e$変化後も増加し続け、その後最終的に復元する。

【００２９】所与のレギュレータに対する勾配値ｍは、その構成によって左右される。一般的に、ｍは次のようにして確定する。

１）ΔI_{load}に等しい負荷電流のステップ増加に対して、出力負荷および出力コンデンサの並列結合に向けて電圧レギュレータが注入する電流の最大可用勾配の絶対値を決定する。

２）ΔI_{load}に等しい負荷電流のステップ減少に対して、出力負荷および出力コンデンサの並列結合に向けて注入される電流の最小可用勾配の絶対値を決定する。負荷電流におけるステップ状減少の結果、注入電流は負の勾配を有することになる。このステップに対して、次に、「負荷電流におけるステップ状減少に対する．．．最大可用勾配」は最大の負の勾配に等しくなる。

３）２つの絶対値の内どちらの方が小さいのかについて判定を行う。これは、「最悪事態」の最大可用勾配である。２つの絶対値の内小さい方が値ｍとなり、ここで求めた式において用いられる。

【００３０】スイッチング・レギュレータでは、最悪事態の最大可用勾配ｍは、明らかに、その入力電圧V_{in}、その出力電圧V_{out}、およびその出力インダクタのインダクタンスＬによって定義される。例えば、バック型電圧レギュレータ（ｂｕｃｋ？ｔｙｐｅ　ｖｏｌｔａｇｅ　ｒｅｇｕｌａｔｏｒ）では、ｍは、以下のように決めることができる。V_{out}が$V_{in}-V_{out}$未満である場合、ｍは$m=V_{out}/L$で与えられる。V_{out}が$V_{in}-V_{out}$よりも大きい場合、ｍは$m=(V_{in}-V_{out})/L$で与えられる。

【００３１】線形電圧レギュレータでは、最悪事態最大可用勾配は、そう明確には定義されない。これは、その電圧誤差増幅器の補償、その半導体デバイスの物理的特性、および可能性として負荷電流の値も含む、多数の要因に依存する。

【００３２】本発明によって達成可能な２つの最適な負荷過渡応答を図６および図７に示す。図６ａは、出力コンデンサの容量ＣがC_{crit}以上の場合に、適正に構成されたレギュレータについて、図６ｂに示す負荷電流における双方向ステップに対する最適な負荷過渡応答を示す。ＣはC_{crit}以上であるので、最大出力電圧偏差は$R_e*\Delta I_{load}$に制限される。図７ａは、適正に構成されたレギュレータの出力コンデンサの容量がC_{crit}未満の場合に、図７ｂの負荷電流における双方向ステップ変化ΔI_{load}に対する最適負荷過渡応答を示す。コンデンサのR_eによって生ずる初期ステップ（$=R_e*\Delta I_{load}$）の後、V_{out}は徐々に定常状態値に向かって傾斜し、次いで、負荷電流がステップ状に低下して元に戻るまで、定常状態値において一定に留まる。この場合のピーク電

圧偏差ΔV_{out}は、次の式で与えられることを示すことができる。

$$\Delta V_{out} = \Delta I_{load}^2 / 2mC + mCR_e^2 / 2 \quad \text{（式２）}$$

ここで、mおよびΔI_{load}は、式１におけると同一であり、CおよびR$_e$は、それぞれ、用いる出力コンデンサの容量およびＥＳＲである。本発明は、C_{crit}未満の容量を有するコンデンサを用いなければならない場合であっても、なおも式２によって与えられるピーク電圧偏差を超過しないことを保証する方法を提供する。したがって、ここで用いる場合、C_{crit}よりも大きな容量の出力コンデンサを有するレギュレータに対する「最適応答（ｏｐｔｉｍｕｍ　ｒｅｓｐｏｎｓｅ）」は、図６ａに示すようなものであり、レギュレータは、サイズΔI_{load}の負荷電流ステップに応答し、初期出力電圧偏差は$\Delta I_{load} * R_e$に等しく、次の負荷電流ステップまで一定に留まる。出力コンデンサの容量がC_{crit}未満の場合、最適応答は図７ａに示すようになり、ピーク出力電圧偏差は式２で与えられ、次の負荷電流ステップまで一定に留まる。

【００３４】一旦mの値を所与のレギュレータに対して決定したなら、最適応答が得られる最小サイズのコンデンサ（図６ａまたは図７ａによる）を決定することができる。最小サイズのコンデンサは、以下の式を満足する容量CおよびＥＳＲ　R$_e$の組み合わせを有するものである。

【００３５】

$$C_{min} = [\Delta I_{load}^2 / 2m + mT_c^2 / 2] / \Delta V_{out} \quad \text{（式３）}$$

ここで、mは先に計算した勾配値、ΔV_{out}はΔI_{load}に等しい負荷電流のステップ変化に対する最大許容電圧偏差、そしてT$_c$は特性時定数（以下で論ずる）である。

【００３６】所与のコンデンサの種類に対して、式３を満足する最小サイズが存在する。コンデンサの種類には、例えば、アルミニウム（Ａｌ）電解質コンデンサ、セラミック・コンデンサ、およびＯＳ-ＣＯＮ（有機半導体電解質を有するＡｌ）コンデンサが含まれる。出力コンデンサの種類の選択は、多数の要因によって影響される。スイッチング・レギュレータでは、重要な考慮点の１つは、スイッチング周波数である。低周波数の設計（例えば、２００ｋＨｚ）では、Ａｌ電解質コンデンサを使用する傾向があり、中間周波数設計（例えば、５００ｋＨｚ）ではＯＳ？ＣＯＮコンデンサを使用する傾向があり、高周波数設計（１ＭＨｚ以上）ではセラミック・コンデンサを使用する傾向がある。

【００３７】一旦コンデンサの種類を選択したなら、その特性時定数T$_c$を決定する。これは、そのＥＳＲおよびその容量の積によって与えられる。コンデンサのＥＳＲは、その容量が増大すると減少する傾向があるので、T$_c$は、所与の種類および電圧定格のコンデンサに対してはほぼ一定となる傾向がある。例えば、標準的な低電圧（例えば、１０Ｖ）Ａｌ電解質コンデンサは、約４０μｓ（例えば、２ｍＦｘ２０ｍΩ）の特性時定数を有し、セラミック・コンデンサは約１００ｎｓ（例えば、１０μＦｘ１０ｍΩ）の特性時定数を有し、ＯＳ-ＣＯＮコンデンサは約４μｓ（例えば、１００μＦｘ４０ｍΩ）の特性時定数を有する。

【００３８】選択したコンデンサの種類に対して決定したT$_c$を用いて、式３にしたがって最小容量を確定する。最小ＥＳＲ　R$_{e(max)}$は次の式で与えられる。

【００３９】

$$R_{e(max)} = T_c / C_{min}$$

※【００３３】

※　【数１２】

※【数１３】

C_{min}に等しい、または好ましくはこれよりも大きい容量C、およびR$_{e(max)}$に等しいまたは好ましくはこれよりも多少小さいＥＳＲ　R$_c$を有するコンデンサを、レギュレータの出力コンデンサとして用いる。Cが先に計算したC_{crit}値以上の場合、図６ａによる応答が得られる。CがC_{crit}未満の場合、図７ａのような応答が達成される。C_{min}に等しい容量およびR$_{e(max)}$に等しいＥＳＲを有する出力コンデンサを用いることは、許容可能であるが、推奨しない。こうすると、実用上稚拙な設計となり、許容範囲、経年変化、温度等に対する安全マージンが得られない。一方、R$_{e(max)}$よりもかなり小さめのＥＳＲを有するコンデンサを選択することも推奨しない。何故なら、コンデンサはＥＳＲが小さい程、コスト高となる傾向があるからである。一旦出力コンデンサのＥＳＲ値を確定したなら、その容量Cはほぼコンデンサの種類の選択によって決定されることを注記しておく。したがって、CはC_{crit}よりもかなり大きくなる場合もあるが、選択したコンデンサ種類の範囲内では、コンデンサのサイズは依然として最小のままである。

【００４０】出力コンデンサを選択した後、電圧レギュレータは、その応答が図５ａ（$C > C_{crit}$の場合）または図６ａ（$C < C_{crit}$の場合）に示した最適形状を有するように構成する必要がある。$C > C_{crit}$の場合、最適応答を達成するには、電圧レギュレータの出力インピーダンス（出力コンデンサのインピーダンスを含む）が抵抗性となり、出力コンデンサのＥＳＲに等しくなるように、電圧レギュレータを構成する。$C < C_{crit}$の場合、最適応答は、負荷および出力コンデンサの結合に、最大可用勾配で、ピーク偏差に達するまで、レギュレータに電流を注入させることによってのみ保証される。この場合、レギュレータは、この応答の部分に対して非線形モードで動作するので最適出力インピーダンスを定義することはできないか、ほぼ最適な応答が得られるように出力インピーダンスの選択が可能であることには変わりな

い。

【００４１】本発明による電圧レギュレータの一実施形態を図８に示す。可制御電力段５０は、トランスコンダクタンスｇによって特徴付けられ、制御入力５３において受け取る制御信号に応答して、出力ノード５２に出力V_{out}を生成する。電力段５０は負荷５４を駆動する。出力コンデンサ５６が負荷間に並列に接続されており、ここでは、その容量性成分Ｃおよび等価直列抵抗R_e成分に分割して示されている。出力ノード５２と制御入力５３との間に、フィードバック回路５８が接続されている。

【００４２】フィードバック回路５８は、例えば、電圧＊誤差増幅器５９を含むことができ、第１入力６０において出力電圧V_{out}を表わす信号を、第２入力において基準電圧を受け取るように接続され、その入力間の差電圧と共に変動する出力６２を生成する。図８に示す実施形態では、最適負荷過渡応答、即ち、コンデンサ５６がC_{crit}以上の場合には図６ａによる最適負荷過渡応答、そしてコンデンサ５６がC_{crit}未満の場合には図７ａによる最適負荷過渡応答は、その利得Ｋ（ｓ）が次の式で与えられるように、電圧誤差増幅器５９を補償することによって達成される。

【００４３】

【数１５】

$$K(s) = -(1/gR_o)(1/(1+sR_eC)) \quad (式4)$$

ここで、ｇは可制御電力段５０のトランスコンダクタンス、ＣおよびＲｅは、それぞれ、出力コンデンサ５６の容量およびＥＳＲであり、ｓは複素周波数、ならびに※$_o$は次の式で与えられる量である。

【００４４】

【数１６】

$$C \geq C_{crit} \text{の場合、} R_o = R_e \quad (式5)$$

【００４５】

★ ★【数１７】

$$C < C_{crit} \text{の場合、} R_o = (\Delta I_{load}/2mC) + (mCR_e^2/2\Delta I_{load}) \quad (式6)$$

ここで、ＣおよびＲｅは、それぞれ、出力コンデンサ５６の容量およびＥＳＲであり、ｍは出力コンデンサ５６および負荷５４の並列結合に向けて注入される電流の最小勾配の絶対値（C_{crit}の決定に関して論じた通りである）であり、ΔI_{load}はレギュレータが対処するように設計した最大負荷電流ステップである。

【００４６】式５および式６において定義したR_oの値は、レギュレータのピーク電圧偏差の尺度となる。ＣがC_{crit}以上の場合、電圧誤差増幅器５９の利得Ｋ（ｓ）は式４に定義したようになり、レギュレータおよび出力コンデンサ５６の結合出力インピーダンスは、出力コンデンサの等価直列抵抗R_eに等しくなる。したがって、ピーク電圧偏差は、$\Delta I_{load} * R_o$となり、これは、Ｃ≧C_{crit}の場合、$\Delta I_{load} * R_e$に等しい。

【００４７】ＣがC_{crit}未満であり、電圧誤差増幅器５９の利得Ｋ（ｓ）が式４に定義した通りである場合、ピーク電圧偏差ΔV_{out}は、式２に定義したようになる。ＣがC_{crit}未満の場合システムは非線形となり、したがって、レギュレータは図６ａに示す最適過渡応答を達成することができない。しかしながら、電圧誤差増幅器５９を補償して式４で与えられる伝達関数を形成すれば、図６ａの理想的な応答に実際上できるだけ近い過渡応答が得られる。

【００４８】可制御電力段５０は、いずれの特定構成にも限定されるものではない。図８では、電力段５０は、電力モード制御を行うように構成されており、電力段は、R_sに等しいトランスレジスタンスを有し、電力段の出力電流と共に変動する出力信号を生成する電流センサ、電流センサの出力および電圧誤差増幅器の出力６２を入力として受け取り、出力６７を生成する電流コントローラ、および電流コントローラからの出力６７を受け取り、応答して出力電圧V_{out}を生成する電力回路６８を含む。本発明は、線形レギュレータおよびスイッチング・レギュレータ双方に適用可能である。線形レギュレータでは、電力回路６８は直列パス・トランジスタであり、電流コントローラ６６は増幅器である。スイッチング・レギュレータでは、電力回路６８は、制御型スイッチ、ダイオード、インダクタ、変圧器、およびコンデンサのような構成部品を含む、多数のトポロジのいずれでも有することができる。例えば、バック型スイッチング・レギュレータの典型的な電力回路を図１に示す。これは、１対の被制御スイッチ１４および１６、ならびにスイッチとレギュレータの出力との接合部間に接続された出力インダクタＬを含む。

【００４９】スイッチング・レギュレータの電流コントローラ６６には、２つの形式が可能である。即ち、瞬時型および平均型である。瞬時電流制御は、例えば、Ａ．Ｓ．Ｋｉｓｌｏｖｓｋｉ（Ａ．Ｓ．キスロブスキ）、Ｒ．Ｒｅｄｌ（Ｒ．レドル）、およびＮ．Ｏ．Ｓｏｋａｌ（Ｎ．Ｏ．ソカル）、Ｄｙｎａｍｉｃ ａｎａｌｙｓｉｓ ｏｆ ｓｗｉｔｃｈｉｎｇ?ｍｏｄｅ ＤＣ／ＤＣ ｃｏｎｖｅｒｔｅｒｓ（スイッチング・モードＤＣ／ＤＣ変換器の動的分析）、Ｖａｎ Ｎｏｓｔｒａｎｄ Ｒｅｉｎｈｏｌｄ（１９９１）、１０２ページに記載されているように、少なくとも６種類の異なる下位形式を有し、一定オフ時間ピーク電流制御、一定オン時間バレー電流制御、ヒステリティック制御（ｈｙｓｔｅｒｅｔｉｃ ｃｏｎｔｒｏｌ）、一定周波数ピーク電流制御、一定周波数バレー電流制御、およびＰＷＭコンダクタンス制御が含まれる。瞬時電流コントローラは、通

常、一スイッチング期間内で出力インダクタにおける電流を変化させることができるが、平均電流制御によってインダクタ電流を変化させるには通常数期間を要する。この理由のために、瞬時電流制御の方が好ましいが、平均電流コントローラも、電流制御ループが十分に速い応答を有するのであれば、本発明を実現するために使用可能である。しかしながら、かかる実施態様は、電流誤差増幅器を必要とするという欠点があり、レギュレータ回路の複雑度およびコストの上昇を招く。

【００５０】図９は、本発明によるスイッチング電圧レギュレータの可能な一実施形態の概略図である。この実施形態では、フィードバック回路５８が電圧誤差増幅器５９を含み、電圧誤差増幅器５９は、演算増幅器７０、入力抵抗器R_1、フィードバック抵抗器R_2、およびフィードバック・コンデンサC_1で構成されている。電力回路６８は、V_{in}および接地間に接続された１対のスイッチ７２および７４を含み、これらのスイッチ間の接合部は出力インダクタＬに接続されている。電流センサ６４が、抵抗R_sを有する抵抗器７５によって実現され、インダクタＬおよび出力ノード５２の間に直列に接続されている。

【００５１】電流コントローラ６６は、一定オフ時間ピーク電流制御型コントローラであり、電圧比較器７６を含む。電圧比較器７６の入力は、抵抗器７５のインダクタ側、および加算回路７８の出力に接続されている。加算回路７８は、その出力Ｚに、そのＸおよびＹ入力の電圧の和に等しい電圧を生成する。Ｘは電圧誤差増幅器５９の出力６２を受けるように接続され、Ｙは電流検知抵抗器７５の出力側に接続されている。また、加算回路７８は、固定利得ｋを有し、電圧誤差増幅器５９の出力およびそのＸ入力間に接続された、利得段８０を有する。利得ｋは、出力電圧V_{out}および基準抵抗V_{ref}がほぼ等しいと予想される場合、単位、例えば、０．０１よりも大幅に小さくなければならない。比較器７６の出力は、単安定マルチバイブレータ８２に接続されており、その出力は、論理反転器８４を介して、駆動回路８３に供給される。駆動回路８３は、上位ドライバ８６および下位ドライバ８８を含み、電力回路６８のスイッチ７２および７４をそれぞれ駆動する。

【００５２】図９のスイッチング・レギュレータ回路の動作は次の通りである。インダクタＬ内の電流と抵抗器７５の抵抗R_sの積が、電圧誤差増幅器５９が生成する誤差電圧を超過する場合、電圧比較器７６の出力は高となり、単安定マルチバイブレータをトリガする。論理反転器８４は、マルチバイブレータ８２の高出力を反転し、上位ドライバ８６に上位スイッチ７２をオフに切り＊替えさせ、下位ドライバ８８に下位スイッチ７４をオンに切り替えさせる。その結果、インダクタＬの電流は減少し始める。単安定マルチバイブレータ８２は、関連するタイミング間隔T_{off}を有し、タイミング間隔T_{off}が経過した後、スイッチ７２および７４の状態は逆転し、インダクタＬ内の電流は増加し始める。インダクタ電流が比較器７６のスレシホルドを超過すると、サイクルが繰り返される。出力電圧調整を行うには、加算回路７８により、誤差増幅器５９からの誤差電圧を用いて電圧比較器８２のスレシホルドを変化させる。

【００５３】本発明にしたがって構成すると、図９のスイッチング電圧レギュレータは、図１０ａおよび図１０ｂにそれぞれ示す、負荷電流I_{load}および出力電圧V_{out}のシミュレーション・プロットに示すような、ほぼ最適な負荷過渡応答を得る。この例では、負荷電流は０．５６Ａから１４．５６Ａまで変化し、そして戻り（ΔI_{load}＝１４Ａ）、許容出力電圧偏差ΔV_{out}は０．０７Ｖである。スイッチング・レギュレータのパラメータ値は、次の通りである。

【００５４】V_{in}＝５Ｖ、V_{ref}＝２．８Ｖ、Ｌ＝３μＨ、Ｃ＝１０ｍＦ、R_e＝５ｍΩ、R_s＝５ｍΩ、ｋ＝０．０１、ΔI_{load}＝１４Ａ、ΔV_{out}＝０．０７Ｖ。

【００５５】出力コンデンサのＲｅは、$R_{e(max)}=\Delta V_{out}/\Delta I_{load}$によって定義される容認範囲内であり、ここでは、０．０７Ｖ／１４Ａ＝５ｍΩに等しいことを注記しておく。

【００５６】この例では、V_{out}（＝V_{ref}）は、V_{in}＝V_{out}より大きいので、ｍは以下の式で与えられる。

【００５７】

【数１８】ｍ＝（$V_{in}-V_{out}$）／Ｌ＝［（５－２．８）Ｖ］／３μＨ＝０．７３３Ａ／μｓ

式１から、クリティカル容量C_{crit}は、次の式で与えられる

【００５８】

【数１９】C_{crit}＝１４Ａ／［（０．７３３Ａ／μｓ）（５ｍΩ）］＝３．８１８ｍＦ

１０ｍＦは３．８１４ｍＦよりも大きいので、ＣはC_{crit}よりも大きく、したがってＲ。（式５で与えられる）はR_eに等しくなる。これを達成するには、電圧誤差増幅器５９を必要に応じて補償し、式４の伝達関数を得る。電圧誤差増幅器５９を図９に示すように実現する場合、以下の２つの式を満足すれば、この補償は行われる。

【００５９】

【数２０】

$$K*(R_2/R_1)=1/(g*R_e) \quad (式7)$$

【００６０】※　※【数２１】

$$R_e*C=R_1*C_1 \quad (式8)$$

ｇの値は、電流センサ６４のトランスレジスタンスおよび電流コントローラ６６の実施態様によって決定され

る。電流コントローラの第１段が電圧比較器（この場合のように）である場合、ｇは電流センサ６４のトランスレジスタンスの逆に等しい。電流センサを抵抗で実現する場合、トランスレジスタンスは単に抵抗器の抵抗となる（したがって、この例では、ｇ＝１／Ｒｓ）。この例では、以下の成分値を用いた場合に、式７および式８を満足する。

【００６１】

Ｒ１＝１ｋΩ、Ｒ２＝１００ｋΩ、Ｃ１＝５００ｐＦ

図１０ｂの波形が示すように、出力電圧応答は、５ｍΩの抵抗性出力インピーダンスに対応し、出力コンデンサのＥＳＲにも等しい。

【００６２】フィードバック回路５８の一代替実施態様を図１１に示す。ここでは、電圧誤差増幅器５９は、トランスコンダクタンス増幅器９０を用いて実現している。トランスコンダクタンス増幅器は、出力電流が、非反転入力および反転入力間の電圧差に比例することを特徴とする。出力電流および入力差電圧間の比例係数は、増幅器のトランスコンダクタンスｇｍとなる。トランスコンダクタンス型電圧誤差増幅器の電圧利得は、トランスコンダクタンス増幅器９０の出力に接続されているインピーダンスと、トランスコンダクタンスｇｍとの積に等しい。

【００６３】図９および図１１に示す電圧誤差増幅器の実施態様は、以下の３つの式を満足する場合、等価となる。

【００６４】

【数２２】

$$g_m [(R_3 R_4) / (R_3 + R_4)] = R_2 / R_1 \qquad \text{式９}$$

【００６５】

※　※【数２３】

$$V_{cc} [(R_4) / (R_3 + R_4)] = V_{ref} \qquad \text{式１０}$$

【００６６】

★　★【数２４】

$$C_2 [(R_3 R_4) / (R_3 + R_4)] = C_1 R_2 \qquad \text{式１１}$$

したがって、式９、式１０および式１１の各々を満足すると、式４に定義した伝達関数が、図１１に示す電圧誤差増幅器５９について得られる。

【００６７】本発明は、電圧誤差増幅器を含む電流モード制御型電圧レギュレータと共に用いることに限定される訳ではない。電流モード制御も電圧誤差増幅器も使用しない本発明の可能な一実施形態を図１２に示す。この実施形態では、可制御電力段１００が、１対の入力１０２、１０４間の電圧差に応じて出力電圧Ｖｏｕｔを生成する。電力段は、入力を受け取る高速電圧コントローラ１０５によって制御される電力回路６８を含む。スイッチング電圧レギュレータでは、高速電圧コントローラ１０５は、知覚し得る正の電圧差が入力１０２および１０４間に現れた場合に、その出力におけるパルス列のデューティ比を急速に大きくするという特徴がある。線形電圧レギュレータでは、高速電圧コントローラ１０５は、通常、広帯域演算増幅器を用いて実現する。

【００６８】また、図１２の実施形態は、電力段１００☆の出力と出力ノード５２との間に直列に接続されたトランスレジスタンスＲｓを有する電流センサ１０６も含み、レギュレータの出力電流と共に変動する出力を生成する。電流センサの出力は、加算回路１０８の一方の入力に接続され、加算回路の第２入力は出力ノード５２に接続されている。加算回路は、その入力の和に等しい出力電圧を生成し、電力段１００の入力１０２に接続する。

$$Z2/Z1 = [(R_e (1 + s R_e C) - R_s] / R_s \qquad \text{（式１２）}$$

ここで、Ｒｅは式５および式６で定義されており、Ｒｓは電流センサ１０６の抵抗であり、ＲｅおよびＣは採用する出力コンデンサ５６のＥＳＲおよび容量である。

【００６９】電力段１００の入力１０４は、１対のインピーダンスＺ１およびＺ２間の接合点に位置するノード１１０に接続されている。インピーダンスＺ１およびＺ２は、出力ノード５２および電圧基準１１２間に直列に接続されている。レギュレータを図１２に示すように構成する場合、２つのインピーダンスの比Ｚ２／Ｚ１を次の式にしたがって調整することによって、最適過渡応答が得られる。

【００７０】

【数２５】

【００７１】図１２の電圧レギュレータの実施形態の一実施態様を図１３に示す。高速電圧コントローラ１０５は、ヒステレティック比較器（ｈｙｓｔｅｒｅｔｉｃ　ｃｏｍｐａｒａｔｏｒ）１３０によって実現され、その出力は駆動回路１３２に接続されている。駆動回路１３２は、上位ドライバ１３４および下位ドライバ１３６を含む。電力回路６８は、上位スイッチ１３８および下位スイッチ１４０を含み、それぞれ、ドライバ１３４および１３６によって駆動される。出力インダクタしは、スイッチ間の接合部に接続されている。ヒステレティック比較器１３０は、出力電圧を監視し、出力電圧が比較器の上側スレシホルドを超過したときに、上位スイッチをオフにする。上位スイッチは、出力電圧が比較器の下側スレシホルド未満に低下したときに、再びオンになる。

【００７２】電流センサ１０６および加算回路１０８は、抵抗器Ｒｓを有する直列抵抗器１４２によって実現されている。インピーダンスＺ１は、コンデンサＣｅおよび抵抗器Ｒｅの並列結合によって実現され、インピーダンスＺ２は抵抗Ｒｆによって実現されている。

【００７３】図１３のスイッチング・レギュレータの出力インピーダンスが抵抗Ｒｅに等しくなるためには、抵

抗器R_eおよびR,の抵抗比は、次の式で与えられなければならない。

【００７４】

【数２６】$R_7/R_e=(R_e-R_s)/R_s$更に、コンデンサC_tの容量と抵抗器R_eの抵抗の積は、次の式で与えられなけれ
ばならない。

【００７５】

【数２７】$C_tR_e=C[(R_eR_e)/R_s]$

電圧レギュレータの設計技術における当業者には容易に認められるであろうが、先に論じた電圧レギュレータの実施態様および実施形態は、単に例示に過ぎない。多くの他の回路構成を用いても、本発明の方法をここに記載するように実施する限り、最適な過渡応答、および可能な限り最小の出力コンデンサという本発明の目標を達成することができる。

【００７６】ここに記載した本発明の方法は、一般的な設計手順として提示することができ、線形およびスイッチング電圧レギュレータ双方の設計に適用可能であり、先に定義したクリティカル容量を超える容量を有する出力コンデンサおよびこれ未満の容量を有する出力コンデンサ双方の使用にも対応する。この設計手順は、以下のステップにしたがって実施することができる。

【００７７】１．負荷電流におけるステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内に規制出力電圧を維持するために必要な電圧レギュレータの出力コンデンサとして用いられるコンデンサの種類（Ａｌ電解質、セラミック、およびＯＳ－ＣＯＮコンデンサ等）の種類を選択する。

【００７８】２．選択したコンデンサの種類に対して、特性時定数T_cを決定する。これは、先に説明したように、そのＥＳＲおよびその容量の積として定義される。

【００７９】３．ΔI_{load}に等しい負荷電流のステップ状増大に対して、出力負荷および出力コンデンサの並列結合に向けて電圧レギュレータが注入する電流の最大可用勾配の絶対値、ならびにΔI_{load}に等しい負荷電流のステップ状減少に対して、出力負荷および出力コンデンサの並列結合に向けて注入する電流の最小可用勾配の絶対値を決定する。これは、式１に関して説明したように行う。

【００８０】４．２つの絶対値の内小さい方を決定する。小さい方の絶対値をｍとして識別する。

【００８１】５．以下の式にしたがって第１容量C_eを決定する。

【００８２】

【数２８】

$C_e=[\Delta I_{load}^2/2m+mT_c^2/2]/\Delta V_{out}$

６．以下の式にしたがって抵抗R_{e0}を決定する。

【００８３】

【数２９】$R_{e0}=T_c/C_e$

７．以下の式にしたがって、クリティカル容量値C_{crit}を決定する。

【００８４】

【数３０】$C_{crit}=\Delta I_{load}/mR_{e0}$

８．$C_e<C_{crit}$の場合、C_eにほぼ等しい容量C_1、およびR_{e0}にほぼ等しい等価直列抵抗R_{e1}を有する出力コンデンサを用いる。

【００８５】$C_e\geq C_{crit}$の場合、$\Delta V_{out}/\Delta I_{load}$にほぼ等しい等価直列抵抗$R_{e2}$、および$T_c/R_{e0}$にほぼ等しい容量$C_2$を有する出力コンデンサを用いる。

【００８６】９．以下の式にしたがって、抵抗R_eを決定する。$C_e<C_{crit}$の場合、

【００８７】

【数３１】$R_e=\Delta I_{load}/2mC_1+[mC_1(R_{e1})]/2\Delta I_{load}$

$C_e\geq C_{crit}$の場合、

【００８８】

【数３２】$R_e=R_{e2}$

１０．使用する出力コンデンサへの接続の前に定義される、電圧レギュレータの出力インピーダンスが、抵抗R_eおよびインダクタンスL_eの直列結合にほぼ等しくなるように電圧レギュレータを調整する。L_eは次の式で与えられる。

【００８９】$C_e<C_{crit}$の場合、

【００９０】

【数３３】$L_e=C_1*R_{e1}*R_e$

$C_e\geq C_{crit}$の場合、

【００９１】

【数３４】$L_e=C_2*R_{e2}*R_e$

このステップは、前述の方法にしたがってレギュレータのフィードバック回路の伝達関数を式４に対応させることによって、実行する。

【００９２】時定数T_c（またはその構成係数ＣおよびR_e）は、個々のコンデンサ種に対して正確に定義された量ではないことを注記しておく。製造許容誤差、ケース・サイズ、温度および電圧定格を含む多数の要因が全てT_cに影響を及ぼし得る。したがって、実際の設計では、計算に用いたパラメータT_cは、近似値として見なすべきであり、設計手順をある回数繰り返すことが必要な場合もある。

【００９３】また、本発明の方法は、特に電流モード制御を採用するバック型スイッチング電圧レギュレータの設計を対象とする手順として提示することができる。これは、レギュレータの出力コンデンサのサイズを最小に抑えつつ、負荷電流のステップ変化ΔI_{load}に対して指定された電圧偏差仕様ΔV_{out}以内にその出力電圧V_{out}を維持することを保証する。この種のレギュレータは、入力電圧V_{in}および接地間に直列に接続された１対のスイッチを有し、スイッチ間の接合部が出力インダクタに接続されている。スイッチは、インダクタをV_{in}および

接地に交互に接続するように駆動される。以下の設計手順は、$C > C_{crit}$の場合にのみ適用可能であり、その場合、図６ａに示した最適負荷過渡応答が得られることを注記しておく。また、電流モード制御を採用するバック型レギュレータも、前述の設計手順に従うことによって、C_{crit}未満の容量を有する出力コンデンサを使用することが可能であり、これによって、図７ａに示した最適応答を達成することができる。$C > C_{crit}$の場合に適用可能な設計手順は、以下のステップによって実施することができる。

【００９４】１．以下の式にしたがって、レギュレータの出力コンデンサに対して、最大等価直列抵抗$R_{e(max)}$を計算する。

【００９５】

【数３５】$R_{e(max)} = \Delta V_{out} / \Delta I_{load}$

２．以下の式にしたがって、レギュレータの出力インダクタに対する最小インダークタンスL_{min}を決定する。

【００９６】

【数３６】

$L_{min} = (V_{out} T_{off} R_{e(max)}) / V_{ripple\text{-}p\text{-}p}$

ここで、T_{off}は出力インダクタをV_{in}に接続するスイッチのオフ時間、$V_{ripple\text{-}p\text{-}p}$は最大許容ピーク対ピーク出力リップル電圧である。

【００９７】３．L_{min}以上のインダクタンスＬ１を有する出力インダクタを用いる。

４．以下の式にしたがって、出力コンデンサの最小容量C_{min}を決定する。

【００９８】

【数３７】$V_{out} < (V_{in} - V_{out})$の場合、$C_{min} = \Delta I_{load} / [R_{e(max)} (V_{out} / L1)]$

【００９９】

【数３８】$V_{out} > V_{in} - V_{out}$の場合、$C_{min} = \Delta I_{load} / [R_{e(max)} ((V_{in} - V_{out}) / L1)]$

５．C_{min}にほぼ等しい容量Ｃを有する出力コンデンサ、および$R_{e(max)}$にほぼ等しい等価直列抵抗R_eを用いる。

【０１００】６．レギュレータの出力インピーダンスをR_eにほぼ等しくなるように構成する。このステップは、前述の方法にしたがって、レギュレータのフィードバック回路の伝達関数を式４と対応付けさせることによって行う。

【０１０１】以上本発明の特定的な実施形態について示しかつ説明したが、当業者には多数の変形や代替実施形態も想起されよう。例えば、バック型スイッチング・レギュレータのありふれた代替実施形態の１つに、第２スイッチを整流ダイオードで置換したものもある。したがって、本発明は添付した請求の範囲に関してのみ制限されることを意図するものとする。

【図面の簡単な説明】

【図１】従来技術のスイッチング電圧レギュレータ回路の概略図である。

【図２】図２ａおよび図２ｂから成り、それぞれ、出力端子および出力コンデンサ間に接続された抵抗器を含まない従来技術の電圧レギュレータ回路の出力電圧および負荷電流のプロットである。

【図３】図３ａおよび図３ｂから成り、それぞれ、出力端子および出力コンデンサ間に接続された抵抗器を含む従来技術のレギュレータ回路の出力電圧および負荷電流のプロットである。

【図４】図４ａおよび図４ｂから成り、それぞれ、出力電圧が上方向負荷電流ステップに応答して静定する前に負荷電流がステップ状に低下する場合の従来技術の電圧レギュレータ回路の出力電圧および負荷電流のプロットである。

【図５】図５ａないし図５ｅから成り、図５ａは、負荷電流におけるステップ変化のプロットであり、図５ｂは、図５ａに示す負荷電流におけるステップ状変化に応答して、出力コンデンサおよび出力負荷の並列結合に向けて電圧レギュレータによって注入される出力電流のプロットであり、図５ｃは、図５ａに示す負荷電流におけるステップ状変化に応答した電圧レギュレータの出力コンデンサ電流のプロットであり、図５ｄは、出力コンデンサの容量がクリティカル容量C_{crit}よりも大きい場合の、電圧レギュレータの出力電圧のプロットであり、図５ｅは、出力コンデンサの容量がクリティカル容量C_{crit}未満である場合の、電圧レギュレータの出力電圧のプロットである。

【図６】図６ａおよび図６ｂから成り、それぞれ、クリティカル容量C_{crit}以上である出力容量を採用した本発明による電圧レギュレータの出力電圧および負荷電流のプロットである。

【図７】図７ａおよび図７ｂから成り、それぞれ、クリティカル容量C_{crit}未満の出力容量を採用した本発明による電圧レギュレータの出力電圧および負荷電流のプロットである。

【図８】本発明による電圧レギュレータの一実施形態のブロック／概略図である。

【図９】図８に示す電圧レギュレータの実施形態に可能な一実施態様の概略図である。

【図１０】図１０ａおよび図１０ｂから成り、それぞれ、図９による電圧レギュレータに対する出力電圧および負荷電流のシミュレーション・プロットである。

【図１１】図９に示す電圧誤差増幅器の代替実施態様の概略図である。

【図１２】本発明による電圧レギュレータの別の実施形態のブロック／概略図である。

【図１３】図１２に示す電圧レギュレータの実施形態に可能な一実施態様の概略図である。

【符号の説明】

１０　スイッチング電圧レギュレータ

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１２　　プッシュ・プル・スイッチ
１４，１６　　パワーＭＯＳＦＥＴ
１８　　ドライバ回路
２０　　デューティ比変調回路
２４　　クロック回路
２６　　誤差信号発生回路
２８　　高利得演算増幅器
３０　　出力コンデンサ
３２　　負荷
５０　　可制御電力段
５２　　出力ノード
５３　　制御入力
５４　　負荷
５６　　出力コンデンサ
５８　　フィードバック回路
５９　　電圧誤差増幅器
６４　　電流センサ
６６　　電流コントローラ
６８　　電力回路
７０　　演算増幅器

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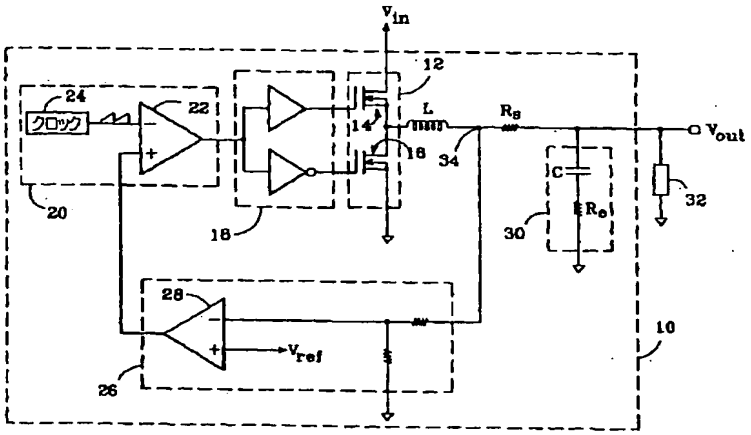
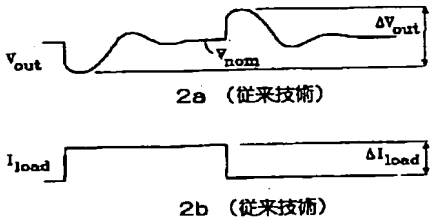
＊７２，７４　　スイッチ
７５　　抵抗器
７６　　電圧比較器
７８　　加算回路
８０　　電力段
８２　　単安定マルチバイブレータ
８３　　駆動回路
８４　　論理反転器
８６　　上位ドライバ
８８　　下位ドライバ
９０　　トランスコンダクタンス増幅器
１００　　可制御電力段
１０５　　高速電圧コントローラ
１０６　　電流センサ
１０８　　加算回路
１３２　　駆動回路
１３４　　上位ドライバ
１３６　　下位ドライバ
１３８　　上位スイッチ
＊１４０　　下位スイッチ

【図１】

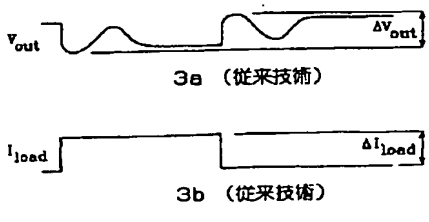


（従来技術）

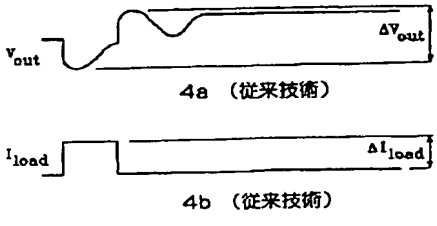
【図２】



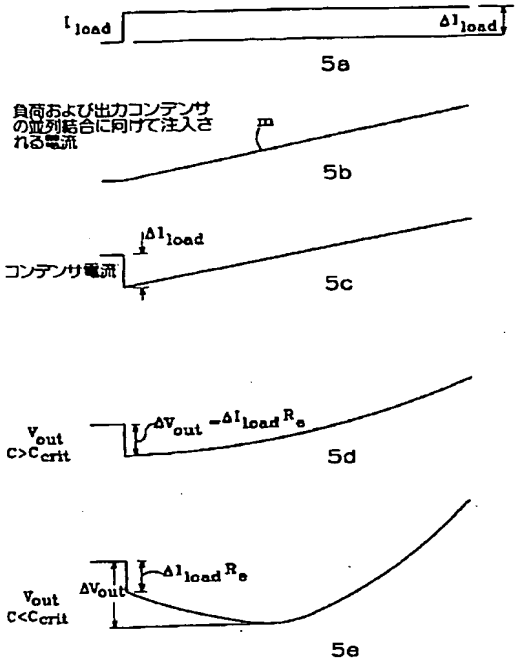
【図３】



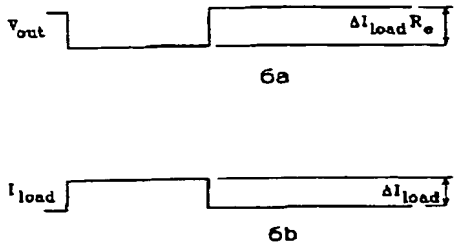
【図４】



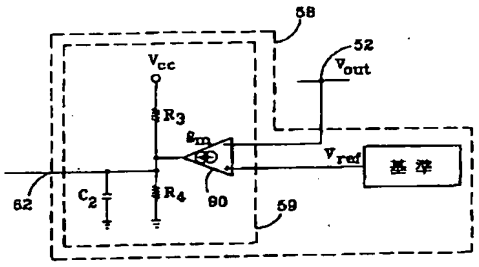
【図５】


I_{load}
ΔI_{load}
5a
負荷および出力コンデンサの並列結合に向けて注入される電流
m
5b
ΔI_{load}
コンデンサ電流
5c
V_{out}
$C>C_{crit}$
$\Delta V_{out} - \Delta I_{load} R_e$
5d
V_{out}
$C<<C_{crit}$
ΔV_{out}
$\Delta I_{load} R_e$
5e

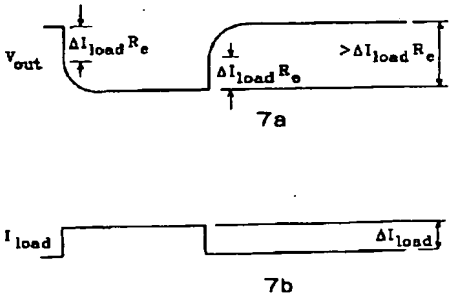
【図６】


V_{out}
$\Delta I_{load} R_e$
6a
I_{load}
ΔI_{load}
6b

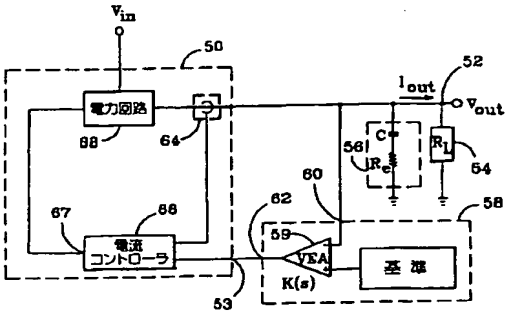
【図９】


58
52
V_{out}
V_{cc}
R_3
g_m
V_{ref}
基準
C_2
R_4
62
90
59

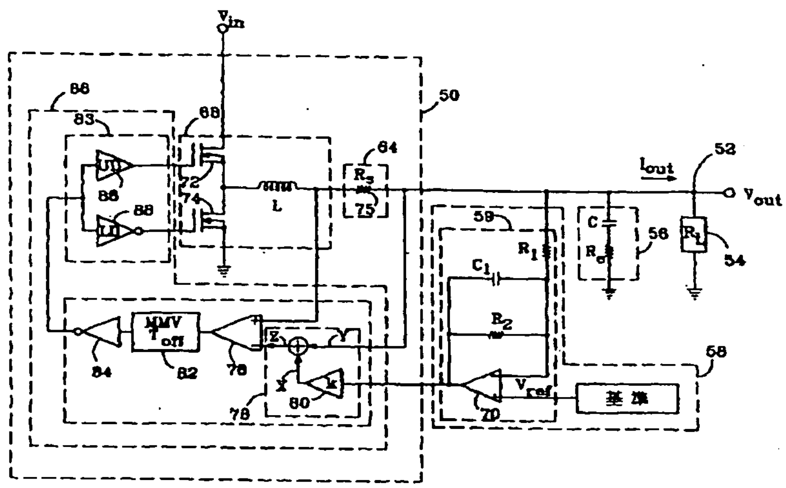
【図７】


V_{out}
$\Delta I_{load} R_e$
$\Delta I_{load} R_e$
$> \Delta I_{load} R_e$
7a
I_{load}
ΔI_{load}
7b

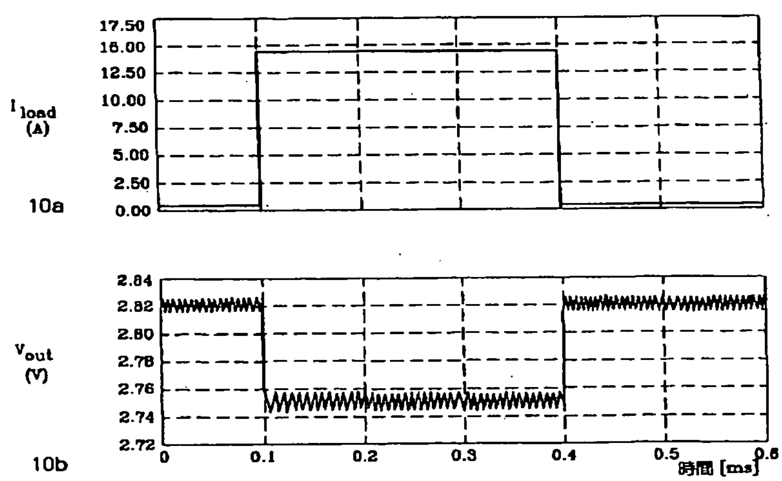
【図８】


V_{in}
50
52
I_{out}
V_{out}
電力回路
68
64
C
ESR
R_L
56
54
60
62
58
67
66
59
電流コントローラ
VEA
基準
K(s)
53

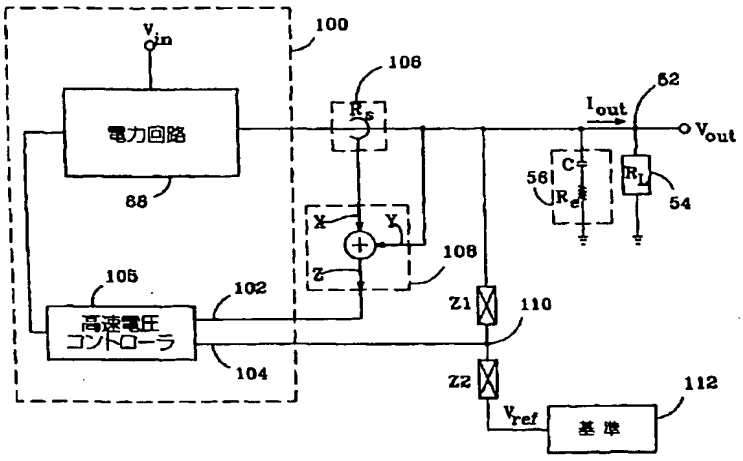
【図１０】


Vin
86
83
68
50
64
52
Iout
Vout
72
74
88
L
Rs
75
59
C1
R1
C
Rc
56
RL
54
R2
MMV
Toff
84
82
76
78
Z
Y
X
k
80
70
Vref
基準
58

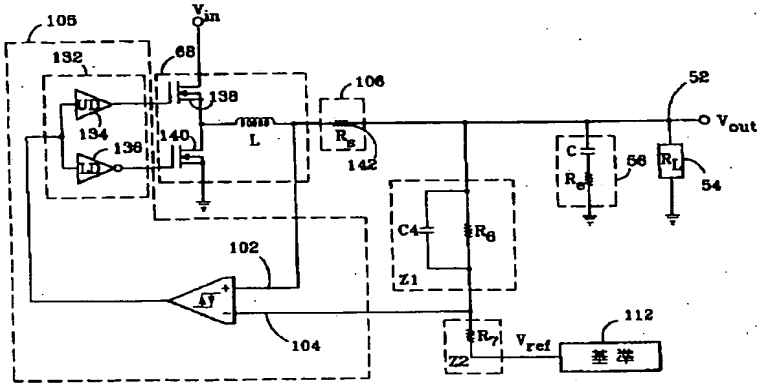
【図１１】


Iload
(A)
10a
17.50
15.00
12.50
10.00
7.50
5.00
2.50
0.00
Vout
(V)
10b
2.84
2.82
2.80
2.78
2.76
2.74
2.72
0
0.1
0.2
0.3
0.4
0.5
0.6
時間 [ms]

【図１２】



【図１３】



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【外国語明細書】

1. Title of Invention

METHOD AND CIRCUIT FOR IMPROVING VOLTAGE REGULATOR LOAD TRANSIENT RESPONSE AND MINIMIZING OUTPUT CAPACITOR SIZE

2. Claims

1. A method of enabling a voltage regulator to employ the smallest possible output capacitor that allows the regulator's output voltage to be maintained within specified boundaries for bidirectional step changes in load current, comprising the step of:

compensating a voltage regulator which employs an output capacitor (56) and is required to maintain a regulated output voltage (V_{out}) within specified boundaries for a bidirectional step change in load current such that its response is flat after its output voltage reaches its peak deviation, the output capacitor required to provide said compensation being the smallest possible output capacitor that allows the regulator's output voltage to be maintained within said specified boundaries.

2. A method of minimizing the size of a voltage regulator's output capacitor which enables the regulator's output voltage to be maintained within a specified voltage deviation specification ΔV_{out} for a bidirectional step change in load current ΔI_{load}, comprising the steps of:

calculating a maximum equivalent series resistance $R_{e(max)}$ for an output capacitor (56) to be employed by a voltage regulator which provides an output voltage (V_{out}) to a load (R_L) at an output node (52), said output capacitor to be connected in parallel across said load, said regulator required to maintain said output voltage within a specified voltage deviation specification ΔV_{out} for a bidirectional step change in load current ΔI_{load}, $R_{e(max)}$ calculated in accordance with the following: $R_{e(max)} = \Delta V_{out}/\Delta I_{load}$,

determining the absolute value of the maximum available slope of the current injected by the voltage regulator toward the parallel combination of the output

load and output capacitor for a step increase in load current equal to ΔI_{load} and the absolute value of the minimum available slope of the current injected toward the parallel combination of the output load and output capacitor for a step decrease in load current equal to ΔI_{load},

determining which of said absolute values is smaller, the smaller of said absolute values being a value m,

determining a critical capacitance C_{crit} in accordance with the following: $C_{crit} = \Delta I_{load}/mR_{e(max)}$,

selecting an output capacitor for connection across said load having an equivalent series resistance R_e that is slightly less than or equal to $R_{e(max)}$ and a capacitance that is greater than or equal to C_{crit}, and

arranging the output impedance of said voltage regulator to be about equal to R_e.

3. The method of claim 2, wherein said voltage regulator includes a controllable power stage (50) which provides the regulator's output voltage in response to a signal received at a control input (53) and a voltage error amplifier (59) connected between said output node and said control input, said power stage characterized by a transconductance g, said step of arranging said output impedance to be about equal to R_e accomplished by making the gain K(s) of said voltage error amplifier equal to the following:

$K(s) = (-1/gR_s)(1/(1+sR_eC))$

in which C and R_e are the capacitance and equivalent series resistance of the output capacitor employed.

4. A method of minimizing the size of a buck-type switching voltage regulator's output capacitor which enables the regulator's output voltage V_{out} to be maintained within a specified voltage deviation specification ΔV_{out} for

a bidirectional step change in load current ΔI_{load}, comprising the steps of:

calculating a maximum equivalent series resistance $R_{e(max)}$ for an output capacitor (56) to be employed by a current-mode controlled switching voltage regulator which receives an input voltage V_{in} and provides an output voltage V_{out} to a load (R_L) connected to an output node (52) via an output inductor (L), said inductor alternately connected to V_{in} and ground via first and second switches (72,74), respectively, said output capacitor to be connected in parallel across said load, said regulator required to maintain V_{out} within a specified voltage deviation specification ΔV_{out} for a bidirectional step change in load current ΔI_{load}, $R_{e(max)}$ calculated in accordance with the following: $R_{e(max)} = \Delta V_{out}/\Delta I_{load}$,

determining a minimum inductance L_{min} for said output inductor in accordance with the following:

$L_{min} = V_{out}T_{off}R_{e(max)}/V_{ripple,p-p}$

where T_{off} is the off time of said first switch and $V_{ripple,p-p}$ is the maximum allowed peak-to-peak output ripple voltage,

selecting an output inductor for use in said regulator having an inductance L1 which is equal to or greater than L_{min},

determining a minimum capacitance C_{min} for said output capacitor in accordance with the following:

$C_{min} = \Delta I_{load}/\{R_{e(max)}(V_{out}/L1)\}$ if $V_{out}<(V_{in}-V_{out})$, and in accordance with the following:

$C_{min} = \Delta I_{load}/\{R_{e(max)}((V_{in}-V_{out})/L1)\}$ if $V_{out} > V_{in} - V_{out}$,

selecting an output capacitor for connection across said load having a capacitance C about equal to C_{min} and an equivalent series resistance R_e about equal to $R_{e(max)}$, and

arranging the output impedance of said regulator to be about equal to R_e.

5. A voltage regulator which maintains its output voltage within a specified voltage deviation specification ΔV_{out} for a bidirectional step change in load current ΔI_{load}, comprising:

a controllable power stage (50) characterized by a transconductance g and connected to produce an output voltage V_{out} at an output node (52) in accordance with a signal received at a control input (53), said output node connected to a load (R_L),

an output capacitor (56) connected to said output node and in parallel across said load, said output capacitor having an equivalent series resistance R_e, and

a voltage error amplifier (59) connected between said output node and said control input, said controllable power stage, said output capacitor and said amplifier forming a voltage regulator required to maintain the voltage at said output node within a specified voltage deviation specification ΔV_{out} for a step change in load current ΔI_{load},

said output capacitor having a capacitance that is equal to or greater than a critical capacitance C_{crit}, in which C_{crit} is given by the following: $C_{crit} = \Delta I_{load}/mR_e$, where m is equal to the smaller of 1)the absolute value of the maximum available slope of the current injected by the voltage regulator toward the parallel combination of the output load and output capacitor for a step increase in load current equal to ΔI_{load}, or 2)the absolute value of the minimum available slope of the current injected by the voltage regulator toward the parallel combination of the output load and output capacitor for a step decrease in load current equal to ΔI_{load}, said voltage regulator arranged to have an output impedance which is about equal to R_e.

6. The voltage regulator of claim 5, wherein the gain K(s) of said voltage error amplifier is given by the

following:

$K(s) = (-1/gR_e)(1/(1+sR_eC))$

where g is equal to the transconductance of said controllable power stage, and R_e and C are equal to the equivalent series resistance and capacitance, respectively, of said output capacitor.

7. The voltage regulator of claim 5, wherein said output capacitor has a capacitance about equal to C_{crit} and an equivalent series resistance R_e about equal to $\Delta V_{out}/\Delta I_{load}$, said capacitor being the smallest possible output capacitor which enables the regulator to maintain its output voltage within ΔV_{out} for a step change in load current ΔI_{load}.

8. A voltage regulator which maintains a regulated output voltage within a specified voltage deviation specification ΔV_{out} for a step change in load current ΔI_{load}, said regulator comprising:

a controllable power stage (100) which provides an output voltage (V_{out}) to a load (R_L) at an output node (52) in accordance with the voltage difference between a first control input (102) and a second control input (104),

an output capacitor (56) connected to said output node and in parallel across said load,

an impedance Z1 connected between said output node and a first node (110),

an impedance Z2 connected between said first node and a reference voltage (V_{ref}),

a current sensor (106) which has a transresistance R_s and produces an output voltage (V_{out}) that varies with the output current (I_{out}) delivered to said load,

a summing circuit (108) which produces an output voltage equal to the sum of the sensor output voltage and the voltage at said output node, said current sensor output

voltage and said summing circuit output voltage connected to said first and second control inputs, respectively, said controllable power stage, said output capacitor, said impedances, said current sensor and said summing circuit forming a voltage regulator required to maintain the voltage at said output node within a specified voltage deviation specification ΔV_{out} for a step change in load current ΔI_{load}, said regulator arranged such that the ratio of impedances Z1 and Z2 is equal to the following:

$Z1/Z2 = [R_o(1+sR_eC)-R_s]/R_e$

where R_e and C are equal to the equivalent series resistance and capacitance, respectively, of said output capacitor, and where R_o is equal to:

R_e, if C is equal to or greater than $\Delta I_{load}/mR_e$,

or to:

$\Delta I_{load}/2mC + (mC(R_e))/2\Delta I_{load}$, if C is less than $\Delta I_{load}/mR_e$,

where m is equal to the smaller of 1)the absolute value of the maximum available slope of the current injected by the voltage regulator toward the parallel combination of the output load and output capacitor for a step increase in load current equal to ΔI_{load}, or 2)the absolute value of the minimum available slope of the current injected by the voltage regulator toward the parallel combination of the output load and output capacitor for a step decrease in load current equal to ΔI_{load}.

9. The voltage regulator of claim 8, wherein said impedance Z1 is implemented with a resistor R1 and a capacitor C1 connected in parallel, and impedance Z2 is implemented with a resistor R2, said resistors R1 and R2 and capacitor C1 arranged such that the output impedance of said voltage regulator is equal to R_o, whereby:

$R2/R1 = (R_o - R_s)/R_s$, and

$C1*R1 = C[(R_oR_e)/R_s]$.

10. The voltage regulator of claim 8, wherein said current sensor and summing circuit comprise a resistor having a resistance R, connected between said controllable output stage at a second node and said output node, the voltage at said second node being said summing circuit output voltage.

3. Detailed Description of Invention

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to the field of voltage regulators, and particularly to methods of improving a voltage regulator's response to a load transient.

Description of the Related Art

The purpose of a voltage regulator is to provide a nearly constant output voltage to a load, despite being powered by an unregulated input voltage and having to meet the demands of a varying load current.

In some applications, a regulator is required to maintain a nearly constant output voltage for a step change in load current; i.e., a sudden large increase or decrease in the load current demanded by the load. For example, a microprocessor may have a "power-saving mode" in which unused circuit sections are turned off to reduce current consumption to near zero; when needed, these sections are turned on, requiring the load current to increase to a high value - typically within a few hundred nanoseconds.

When there is a change in load current, some deviation in the regulator's output voltage is practically unavoidable. The magnitude of the deviation is affected by both the capacitance and the equivalent series resistance (ESR) of the output capacitor: a smaller capacitance or a larger ESR increase the deviation. For example, for a switching voltage regulator (which delivers output current via an output inductor and which includes an output capacitor connected in parallel across the load), a change

in load current (ΔI_{load}) results in a change in the regulator's output voltage unless 1)the current delivered to the load instantaneously increases by ΔI_{load}, or 2)the capacitance of the output capacitor is so large and its ESR is so small that the output voltage deviation would be negligible. The first option is impossible because the current in the output inductor cannot change instantaneously. The time required to accommodate the change in load current can be reduced by reducing the inductance of the output inductor, but that eventually requires increasing the regulator's switching frequency, which is limited by the finite switching speed of the switching transistors and the dissipation in the transistors' driver circuit. The second option is possible, but requires a very large output capacitor which is likely to occupy too much space on a printed circuit board, cost too much, or both.

For applications requiring the regulator's output voltage to meet a narrow load transient response specification, i.e., a specification which narrowly limits the allowable output voltage deviation for a bidirectional step change in load current, this inevitable deviation may be unacceptably large. As used herein, "ΔV_{out}" refers to a regulator's output voltage deviation specification, as well as to peak-to-peak output voltage deviations shown in graphs. The most obvious solution for improving load transient response is to increase the output capacitance and/or reduce the ESR of the output capacitor. However, as noted above, a larger output capacitor (which provides both more capacitance and lower ESR) requires more volume and more PC board area, and thereby more cost.

One approach to improving load transient response is shown in FIG. 1. A switching voltage regulator 10 includes a push-pull switch 12 connected between a supply voltage V_{in} and ground, typically implemented with two synchronously

switched power MOSFETs 14 and 16. A driver circuit 18 is connected to alternately switch on one or the other of MOSFETs 14 and 16. A duty ratio modulator circuit 20 controls the driver circuit; circuit 20 includes a voltage comparator 22 that compares a sawtooth clock signal received from a clock circuit 24 and an error voltage received from a error signal generating circuit 26. Circuit 26 typically includes a high-gain operational amplifier 28 that receives a reference voltage V_{ref} at one input and a voltage representative of the output voltage V_{out} at a second input, and produces an error voltage that varies with the difference between V_{out} and the desired output voltage. The regulator also includes an output inductor L connected to the junction between MOSFETs 14 and 16, an output capacitor 30, shown represented as a capacitance C in series with an equivalent series resistance R_s, and a resistor R_s connected between the output inductor and the output capacitor. V_{out} is connected to drive a load 32.

In operation, MOSFETs 14 and 16 are driven to alternately connect inductor L to V_{in} and ground, with a duty ratio determined by duty ratio modulator circuit 20; the duty ratio varies in accordance with the error voltage produced by error amplifier 28. The current in inductor L flows into the parallel combination of output capacitor 30 and load 32. The impedance of capacitor 30 is much smaller at the switching frequency than that of load 32, so that the capacitor filters out most of the AC components of the inductor current and virtually all of the direct current is delivered to load 32.

Without series resistor R_s, the voltage fed back to circuit 26 is equal to V_{out}, and the regulator's response to a step change in load current is that of a typical switching regulator; a regulator's output voltage V_{out} is shown in FIG. 2a for a step change in load current I_{load}.

shown in FIG. 2b. Because the current in L cannot change instantaneously, a sudden increase in I_{load} causes V_{out} to spike downward; the control loop eventually forces V_{out} back to a nominal output voltage V_{nom}. Similarly, when I_{load} later steps down, V_{out} spikes up before returning to V_{nom}. The total deviation in output voltage ΔV_{out} for a step change in load current is determined by the difference between the two voltage spike peaks. If the regulator is subject to a narrow load transient response specification, this deviation may exceed the tolerance allowed.

Connecting resistor R_s in series with inductor L (at an output terminal 34) can reduce ΔV_{out}; one possible response with R_s included is shown in FIG. 3a for a step change in load current shown in FIG. 3b. With R_s in place, the control loop no longer causes V_{out} to recover to V_{nom}; rather, V_{out} recovers to a voltage given by the voltage at terminal 34 minus the product of ΔI_{load} and R_s. That is, the steady-state value of V_{out} for a light load will be higher than it is for a heavy load, by $\Delta I_{load}*R_s$. Making R_s approximately equal to the ESR of the output capacitor can provide a somewhat narrower ΔV_{out} than can be achieved without the use of R_s.

One disadvantage of the circuit of FIG. 1 is illustrated in FIGs. 4a and 4b. In this case, the load current (FIG. 4b) steps back down before V_{out} (FIG. 4a) has settled to a steady-state value. With V_{out} higher than it was in FIG. 3a at the instant I_{load} falls, the peak of the upward V_{out} spike is also higher, making the overall deviation ΔV_{out} greater than it would otherwise be. This larger deviation means that to satisfy a particular narrow output voltage deviation specification, regulator 10 must use a larger output capacitor that has a proportionally smaller ESR. The cost of a capacitor is approximately inversely proportional to its ESR, so that meeting the specification may be prohibitively expensive.

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Another disadvantage of the FIG. 1 circuit is the considerable power dissipation required of series resistor R_s. For example, assuming an R_s of 5 mΩ and a maximum load current of 14.6 A, the dissipation in R_s will be 1.07 W.

An approach to improving a regulator's load transient response using a different control principle is disclosed in D. Goder and W.R. Pelletier, "V^2 Architecture Provides Ultra-Fast Transient Response in Switch Mode Power Supplies", HFPC Power Conversion, September 1996 Proceedings, pp. 19-23. The regulator described therein includes a push-pull switch, a driver circuit, an error amplifier, and an output inductor and capacitor similar to those shown in FIG. 1. A signal representing the regulator's output voltage is fed to both the error amplifier and to a voltage comparator which also receives the error amplifier's output. When the regulator's output voltage exceeds the output of the error amplifier, the comparator's output goes high and triggers a monostable multivibrator, which turns off the upper switching transistor for a predetermined time interval.

The transient response of this circuit is designed to be faster than that of the circuit in FIG. 1. A load current step immediately changes the voltage at the comparator, bypassing the sluggishness of the error amplifier and thereby shortening the response time. However, even with a shorter response time, the shape of the response trace still resembles that shown in FIG. 3a, with little to no improvement in the magnitude of ΔV_{out}.

Another switching regulator is described in L. Spaziani, "Fueling the Megaprocessor - a DC/DC Converter Design Review Featuring the UC3886 and UC3910", Unitrode Application Note U-157, pp. 3-541 to 3-570. This regulator employs a control principle known as "average current control", in which regulation is achieved by controlling the average value of the current in the output inductor.

A resistor is connected in series with the regulator's output inductor, and a current sense amplifier (CSE) is connected across the resistor to sense the inductor current. The output of the CSE is fed to a current error amplifier along with the output of a voltage error amplifier that compares the regulator's output voltage with a reference voltage. A comparator receives the output of the current error amplifier at one input and a sawtooth clock signal at its other input; the comparator produces a pulse-width modulated output to drive a push-pull switch via a driver circuit.

In operation, an increase in load current causes an output voltage decrease, increasing the error signal from the voltage error amplifier. This increases the output from the current error amplifier, which in turn causes the duty ratio of the pulses produced by the comparator to increase. This increases the current in the output inductor to bring up the output voltage. The voltage error amplifier is configured to provide a non-integrating gain, and this, in combination with average current control, gives the regulator a finite and controllable output resistance. This permits the output voltage to be positioned, similar to the way in which series resistor R, affected the response of the FIG. 1 circuit. However, as is clearly shown in FIG. 32 of the reference, the obtainable response again resembles that of FIG. 3a, with a ΔV_{out} that may still exceed a narrow output voltage deviation specification.

SUMMARY OF THE INVENTION

A method and circuit are presented which overcome the problems noted above, enabling a voltage regulator to provide an optimum response to a large bidirectional load transient while using the smallest possible output capacitor.

The invention is intended for use with voltage regulators for which output capacitor size and cost are preferably minimized, which must maintain its output voltage within specified boundaries for large bidirectional step changes in load current. These goals are achieved by employing an output capacitor that has a combination of the largest possible equivalent series resistance (ESR) and lowest possible capacitance that ensures that the peak-to-peak voltage deviation for a bidirectional step change in load current is no greater than the maximum allowed, and by compensating the regulator to ensure a response that is flat after the occurrence of the peak deviation - referred to herein as an "optimum response". When these conditions are met, the regulator's output capacitor will be the smallest possible capacitor which enables the output voltage to stay within the specified boundaries for a bidirectional step change in load current. The invention is applicable to both switching and linear voltage regulators.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art switching voltage regulator circuit.

FIGs. 2a and 2b are plots of output voltage and load current, respectively, for a prior art voltage regulator circuit which does not include a resistor connected between its output terminal and its output capacitor.

FIGs. 3a and 3b are plots of output voltage and load current, respectively, for a prior art voltage regulator circuit which does include a resistor connected between its output terminal and its output capacitor.

FIG. 11 is a schematic diagram of alternative implementation of the voltage error amplifier shown in FIG. 9.

FIG. 12 is a block/schematic diagram of another embodiment of a voltage regulator per the present invention.

FIG. 13 is a schematic diagram of one possible implementation of the voltage regulator embodiment shown in FIG. 12.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a means of determining the smallest possible capacitor that can be used on the output of a voltage regulator in applications requiring large bidirectional step-like changes in load current, which enables the regulator's output voltage to remain within specified boundaries for a given step size. A given step change in load current is identified herein as ΔI_{load}, and the allowable output voltage deviation specification is identified as ΔV_{out}. As used herein, the "smallest possible output capacitor" refers to the output capacitor having the smallest possible capacitance value and the largest permissible ESR value which enable the regulator to meet the ΔV_{out} specification. Because the cost of a capacitor tends to be inversely proportional to its ESR and directly proportional to its capacitance, and because space is nearly always at a premium on a circuit board, the invention makes it possible for the output capacitor's cost and space requirements to be minimized.

The invention takes advantage of the realization that there is a smallest possible output capacitor that, when used with a properly configured voltage regulator, enables the regulator to meet a given ΔV_{out} specification. Neglecting the effect of the output capacitor's equivalent series inductance, a step change in load current ΔI_{load}

causes an initial change in the output voltage of a voltage regulator that is equal to the product of the capacitor's ESR (identified herein as R_e) and ΔI_{load}; i.e., $R_e*\Delta I_{load}$. This initial change occurs for both upward and downward load current steps. If the output capacitor's capacitance C is equal to or greater than a certain "critical" value C_{crit} (discussed in detail below), the output voltage deviation may not exceed the initial $R_e*\Delta I_{load}$ change. If C is less than C_{crit}, the output voltage deviation continues to increase after the initial $R_e*\Delta I_{load}$ change before beginning to recover.

Prior art regulators are typically designed to drive the output voltage back towards a nominal value after the occurrence of a load transient. Doing so, however, can result in an overall output voltage deviation ΔV_{out} of up to twice $R_e*\Delta I_{load}$: when the load current steps up, V_{out} drops from the nominal voltage by $R_e*\Delta I_{load}$. If the load current stays high long enough, the regulator drives V_{out} back toward the nominal voltage. Now when the load current steps back down, V_{out} spikes up by $R_e*\Delta I_{load}$, resulting in a total output voltage deviation of $2(R_e*\Delta I_{load})$.

Having recognized the adverse implications of prior art regulator control methods on the magnitude of ΔV_{out}, it was realized that an optimum load transient response - i.e., the response that produces the smallest output voltage deviation ΔV_{out} - is a response which remains flat at the upper voltage deviation boundary after a downward load current step, and remains at the lower voltage deviation boundary after an upward load current step. The present invention provides a method of configuring the regulator so that its load transient response is at or near this theoretical optimum. Also realized was that the output capacitor needed to achieve this response is the smallest possible capacitor that can be used to meet the ΔV_{out} specification.

A number of steps must be performed to achieve the goal of providing the optimum response and thereby identifying the smallest possible capacitor which enables a given ΔV_{out} specification to be met. A maximum equivalent series resistance $R_{e(max)}$ is first determined for the output capacitor that will be employed by a voltage regulator subject to a specified voltage deviation specification ΔV_{out} for a bidirectional step change in load current ΔI_{load}. In accordance with Ohm's Law, $R_{e(max)}$ is given by: $R_{e(max)} = \Delta V_{out}/\Delta I_{load}$; if the output capacitor's R_e is any greater than $R_{e(max)}$, the initial deviation in V_{out} for a step change in load current equal to ΔI_{load} is guaranteed to exceed ΔV_{out}.

The next step is to determine the "critical" capacitance value C_{crit} mentioned above. The critical capacitance is the amount of capacitance that, when connected in parallel across a load driven by a voltage regulator (as the regulator's output capacitor), causes the output voltage to have a zero slope - i.e., to become flat after the initial $R_e*\Delta I_{load}$ change - when the current injected by the regulator towards the parallel combination of load and output capacitor ramps up (or down) with the maximum slope allowed by the physical limitations of the regulator. The maximum slope allowed by the physical limitations of the regulator is referred to herein as the "maximum available slope".

The critical capacitance C_{crit} is given by:

$$C_{crit} = \Delta I_{load}/mR_{e(max)} \qquad \text{(Eq. 1)}$$

where ΔI_{load} is the largest expected load current step, $R_{e(max)}$ is the maximum allowable output capacitor ESR (calculated above), and m is a slope value associated with the current injected toward the parallel combination of the output capacitor and output load; m and the method of determining its value are discussed below.

The slope parameter m is illustrated in FIGs. 5a-5c. FIG. 5a depicts the load current waveform for an upward

step. FIG. 5b shows the current injected by the regulator toward the parallel combination of output capacitor and output load when the regulator produces output current at the maximum available slope *m*. FIG. 5c shows the current in the output capacitor, which is equal to the difference between the load current and the injected current.

FIGs. 5d and 5e illustrate how the size of a regulator's output capacitor affects V_{out} when its capacitance C is greater than C_{crit} (FIG. 5d) and less than C_{crit} (FIG. 5e), and the regulator injects a current toward the parallel combination of capacitor and load with the maximum available slope. When $C > C_{crit}$, V_{out} begins to recover immediately after the occurrence of the initial $\Delta I_{load}R_s$ change. However, when $C < C_{crit}$, the output voltage deviation continues to increase after the initial $\Delta I_{load}R_s$ change, before eventually recovering.

The slope value *m* for a given regulator depends on its configuration. In general, *m* is established by:

1) determining the absolute value of the maximum available slope of the current injected by the voltage regulator toward the parallel combination of the output load and output capacitor for a step increase in load current equal to ΔI_{load},

2) determining the absolute value of the minimum available slope of the current injected toward the parallel combination of the output load and output capacitor for a step decrease in load current equal to ΔI_{load}. A step decrease in load current results in an injected current which has a negative slope. For this step, then, the "minimum available slope . . . for a step decrease in load current" is equal to the most negative slope,

3) determining which of the two absolute values is smaller - this is the "worst case" maximum available slope. The smaller of the two absolute values is the value *m* which is to be used in the equations found herein.

In a switching regulator, the worst-case maximum available slope m is clearly defined by its input voltage V_{in}, its output voltage V_{out}, and the inductance L of its output inductor. For example, for a buck-type voltage regulator, m can be determined in accordance with the following: when V_{out} is less than $V_{in} - V_{out}$, m is given by $m = V_{out}/L$. When V_{out} is greater than $V_{in} - V_{out}$, m is given by $m = (V_{in} - V_{out})/L$.

For linear voltage regulators, the worst-case maximum available slope is not as clearly defined. It will depend on a number of factors, including the compensation of its voltage error amplifier, the physical characteristics of its semiconductor devices, and possibly the value of the load current as well.

The two optimum load transient responses achievable with the present invention are depicted in FIGs. 6 and 7. FIG. 6a depicts the optimum load transient response to a bidirectional step in load current shown in FIG. 6b, for a properly configured regulator when the capacitance C of its output capacitor is equal to or greater than C_{crit}. Because C is equal to or greater than C_{crit}, the maximum output voltage deviation is limited to $R_e*\Delta I_{load}$. FIG. 7a shows the optimum load transient response to a bidirectional step change in load current ΔI_{load} in FIG. 7b, when the capacitance of a properly configured regulator's output capacitor is less than C_{crit}. After the initial step ($=\Delta I_{load}*R_e$) caused by the capacitor's R_e, V_{out} gradually declines to a steady-state value, and then remains flat at the steady-state value until the load current steps back down. It can be shown that the peak voltage deviation ΔV_{out} in this case is given by:

$$\Delta V_{out} = \Delta I_{load}^2/2mC + mCR_e^2/2 \qquad \text{(Eq. 2)}$$

where m and ΔI_{load} are the same as in equation 1, and C and R_e are the capacitance and ESR, respectively, of the output capacitor employed. If a capacitor with a capacitance less

than C_{crit} must be used, the invention still provides a method that ensures that the peak voltage deviation given by equation 2 is not exceeded. Thus, as used herein, an "optimum response" for a regulator having an output capacitor with a capacitance greater than C_{crit} is as shown in FIG. 6a, in which the regulator responds to a load current step of size ΔI_{load} with an initial output voltage deviation equal to $\Delta I_{load}*R_e$, and then remaining flat until the next load current step. When the output capacitor has a capacitance less than C_{crit}, an optimum response is as shown in FIG. 7a, with a peak output voltage deviation given by equation 2, and then remaining flat until the next load current step.

Once the value of m has been determined for a given regulator, the minimum size capacitor that provides an optimum response (per FIG. 6a or FIG. 7a) can be determined. The minimum size capacitor is one which has a combination of capacitance C and ESR R_e that satisfies the following equation:

$$C_{min} = [\Delta I_{load}^2/2m + mT_c^2/2]/\Delta V_{out} \quad \text{(Eq. 3)}$$

where m is the slope value calculated above, ΔV_{out} is the maximum allowed voltage deviation for a step change in load current equal to ΔI_{load}, and T_c is a characteristic time constant (discussed below).

For any given capacitor type, there exists a minimum size that satisfies equation 3. Capacitor types include, for example, aluminum (Al) electrolytic capacitors, ceramic capacitors, and OS-CON (Al with an organic semiconductive electrolyte) capacitors. The selection of an output capacitor type is driven by a number of factors. For a switching regulator, one important consideration is switching frequency. Low-frequency designs (e.g., 200 kHz) tend to use Al electrolytic capacitors, medium-frequency designs (e.g., 500 kHz) tend to use OS-CON capacitors, and high-frequency designs (1 MHz and above) tend to use

ceramic capacitors.

Once a capacitor type has been selected, its characteristic time constant T_c is determined, which is given by the product of its ESR and its capacitance. Because a capacitor's ESR tends to decrease as its capacitance increases, T_c tends to be about constant for capacitors of a given type and voltage rating. For example, standard low-voltage (e.g., 10 V) Al electrolytic capacitors have characteristic time constants of about 40μs (e.g., 2mF x 20mΩ), ceramic capacitors have characteristic time constants of about 100ns (e.g., 10μF x 10mΩ), and OS-CON capacitors have characteristic time constants of about 4μs (e.g., 100μF x 40mΩ).

With T_c determined for the selected capacitor type, a minimum capacitance is established in accordance with equation 3. A maximum ESR $R_{e(max)}$ is then given by:
$R_{e(max)} = T_c/C_{min}$.
A capacitor having a capacitance C equal to or preferably, greater than C_{min}, and an ESR R_e equal to or, preferably, slightly less than $R_{e(max)}$ is used as the regulator's output capacitor. If C is equal to or greater than the C_{crit} value calculated above, a response per FIG. 6a is obtained; if C is less than C_{crit}, a response per FIG. 7a is achieved. Using an output capacitor having a capacitance equal to C_{min} and an ESR equal to $R_{e(max)}$ is permissible, but is not recommended. Doing so is a poor design practice which leaves no safety margin against tolerances and changes with age, temperature, etc. On the other hand, selecting a capacitor with an ESR that is much smaller than $R_{e(max)}$ is also not recommended, since a capacitor with a lower ESR tends to cost more. Note that once the output capacitor's ESR value is established, its capacitance C is largely determined by the choice of capacitor type. As such, C may be much greater than C_{crit}, but within the selected capacitor type the size of the capacitor is still minimal.

Having selected the output capacitor, the voltage regulator needs to be configured such that its response will have the optimum shape shown in FIG. 5a (if $C > C_{crit}$) or FIG. 6a (if $C < C_{crit}$). If $C > C_{crit}$, the optimum response is achieved by configuring the voltage regulator such that its output impedance (including the impedance of the output capacitor) becomes resistive and equal to the ESR of the output capacitor. If $C < C_{crit}$, the optimum response is ensured only by forcing the regulator to inject current to the combination of the load and the output capacitor with the maximum available slope until the peak deviation is reached. For this case an optimum output impedance cannot be defined because the regulator operates in a nonlinear mode for part of the response, but the output impedance can still be selected to provide an approximately optimal response.

One embodiment of a voltage regulator per the present invention is shown in FIG. 8. A controllable power stage 50 is characterized by a transconductance g and produces an output V_{out} at an output node 52 in response to a control signal received at a control input 53; power stage 50 drives a load 54. An output capacitor 56 is connected in parallel across the load, here shown divided into its capacitive C and equivalent series resistance R_e components. A feedback circuit 58 is connected between output node 52 and control input 53.

Feedback circuit 58 can include, for example, a voltage error amplifier 59 connected to receive a signal representing output voltage V_{out} at a first input 60 and a reference voltage at a second input, and producing an output 62 which varies with the differential voltage between its inputs. For the embodiment shown in FIG. 8, an optimum load transient response - i.e., per FIG. 6a if capacitor 56 is equal to or greater than C_{crit} and per FIG. 7a is capacitor 56 is less than C_{crit} - is achieved by

compensating voltage error amplifier 59 such that its gain K(s) is given by:

$$K(s) = -(1/gR_o)(1/(1+sR_eC)) \quad \text{(Eq. 4)}$$

where g is the transconductance of the controllable power stage 50, C and R_e are the capacitance and ESR of output capacitor 56, respectively, s is the complex frequency, and R_o is a quantity given by:

$$R_o = R_e, \text{ if } C \geq C_{crit}, \text{ or} \quad \text{(Eq. 5)}$$

$$R_o = (\Delta I_{load}/2mC) + (mCR_e^2/2\Delta I_{load}), \text{ if } C < C_{crit} \quad \text{(Eq. 6)}$$

where C and R_e are the capacitance and ESR of output capacitor 56, respectively, m is the absolute value of the smallest slope of the current injected toward the parallel combination of output capacitor 56 and load 54 (as discussed in connection with the determination of C_{crit}), and ΔI_{load} is the largest load current step which the regulator is designed to accommodate.

The value of R_o defined in equations 5 and 6 is a measure of the peak voltage deviation of the regulator. When C is greater than or equal to C_{crit}, and the gain K(s) of voltage error amplifier 59 is as defined in equation 4, the combined output impedance of the regulator and the output capacitor 56 will be equal to the equivalent series resistance R_e of the output capacitor. Therefore, the peak voltage deviation will be $\Delta I_{load}*R_o$, which is equal to $\Delta I_{load}*R_e$ when $C \geq C_{crit}$.

When C is less than C_{crit}, and the gain K(s) of voltage error amplifier 59 is as defined in equation 4, the peak voltage deviation ΔV_{out} will be as defined in equation 2. The system is nonlinear when C is less than C_{crit}, and as such the regulator cannot achieve the optimal transient response shown in FIG. 6a. However, compensating voltage error amplifier 59 to yield the transfer function given by equation 4 provides a transient response that is as close to FIG. 6a's ideal response as practically possible.

Controllable power stage 50 is not limited to any particular configuration. In FIG. 8, power stage 50 is configured to provide current-mode control; the power stage includes a current sensor 64 which has a transresistance equal to R, and which produces an output signal that varies with the power stage's output current, a current controller 66 which receives the output of the current sensor and the output 62 of the voltage error amplifier as inputs and produces an output 67, and a power circuit 68 which receives output 67 from the current controller and produces output voltage V_{out} in response. The invention is applicable to both linear and switching regulators: in linear regulators, power circuit 68 is a series pass transistor and current controller 66 is an amplifier. For a switching regulator, power circuit 68 can have any of a large number of topologies, containing components such as controlled switches, diodes, inductors, transformers, and capacitors. For example, a typical power circuit for a buck-type switching regulator is shown in FIG. 1, which includes a pair of controlled switches 14 and 16 and an output inductor L connected between the junction of the switches and the regulator's output.

The current controller 66 for a switching regulator can be of two types: instantaneous and average. Instantaneous current control has at least six different subtypes, as described, for example, in A. S. Kislovski, R. Redl, and N. O. Sokal, Dynamic analysis of switching-mode DC/DC converters, Van Nostrand Reinhold (1991), p. 102, including constant off-time peak current control, constant on-time valley current control, hysteretic control, constant frequency peak current control, constant frequency valley current control, and PWM conductance control. Instantaneous current controllers can typically change the current in the output inductor within one switching period, while changing the inductor current with average current

control usually takes several periods. For this reason, instantaneous current control is preferred, but average current controllers can also be used to implement the present invention if the current-controlling loop has sufficiently fast response; however, such implementations suffer from the drawback of requiring a current error amplifier, which increases the complexity and cost of the regulator circuit.

FIG. 9 is a schematic diagram of one possible implementation of a switching voltage regulator per the present invention. In this embodiment, feedback circuit 58 includes voltage error amplifier 59, which is made up of an operational amplifier 70, an input resistor R_1, a feedback resistor R_2, and a feedback capacitor C_1. Power circuit 68 includes a pair of switches 72 and 74 connected between V_{in} and ground, with the junction between the switches connected to an output inductor L. Current sensor 64 is implemented with a resistor 75 having a resistance R_s, connected in series between inductor L and output node 52.

Current controller 66 is a constant off-time peak current control type controller, which includes a voltage comparator 76 with its inputs connected to the inductor side of resistor 75 and to the output of a summing circuit 78. Summing circuit 78 produces a voltage at its output Z that is equal to the sum of the voltages at its X and Y inputs; X is connected to receive the output 62 of voltage error amplifier 59, and Y is connected to the output side of current sense resistor 75. Summing circuit 78 can also include a gain stage 80 having a fixed gain k, connected between the output of voltage error amplifier 59 and its X input; the gain k should be significantly less than unity - e.g. 0.01 - if the output voltage V_{out} and the reference voltage V_{ref} are expected to be nearly equal. The output of comparator 76 is connected to a monostable multivibrator 82, the output of which is fed to a driving circuit 83 via

a logic inverter 84. Driving circuit 83 includes upper driver 86 and lower driver 88, which drive switches 72 and 74, respectively, of power circuit 68.

The operation of the switching regulator circuit of FIG. 9 is as follows: when the product of the current in inductor L and the resistance R_s of resistor 75 exceeds the error voltage produced by voltage error amplifier 59, the output of voltage comparator 76 goes high and triggers monostable multivibrator 82. Logic inverter 84 inverts the high output of multivibrator 82, which causes upper driver 86 to turn off upper switch 72 and lower driver 88 to turn on lower switch 74. As a result, the current in inductor L begins to decrease. Monostable multivibrator 82 has an associated timing interval T_{off}; after timing interval T_{off} has expired, the states of switches 72 and 74 reverse, and the current in inductor L begins to increase. When the inductor current exceeds the threshold of comparator 76, the cycle repeats. Output voltage regulation is achieved by changing the threshold of voltage comparator 82 with the error voltage from error amplifier 59 via summing circuit 78.

When configured per the present invention, the switching voltage regulator of FIG. 9 provides a nearly optimum load transient response, as illustrated in the simulated plots of load current I_{load} and output voltage V_{out} shown in FIGS. 10a and 10b, respectively. In this example, the load current changes from 0.56 A to 14.56 A and back (ΔI_{load} = 14 A) and the allowable output voltage deviation ΔV_{out} is 0.07 V. The parameter values of the switching regulator are as follows:

V_{in} = 5 V; V_{ref} = 2.8 V; L = 3 μH; C = 10 mF; R_e = 5 mΩ; R_s = 5 mΩ; k = 0.01; ΔI_{load} = 14 A; ΔV_{out} = 0.07 V

Note that the output capacitor's R_e is within the acceptable range defined by $R_{e(max)}=\Delta V_{out}/\Delta I_{load}$, equal here to 0.07V/14A = 5 mΩ.

For this example, V_{out} ($=V_{ref}$) is greater than $V_{in} - V_{out}$, so that m is given by:

$m = (V_{in} - V_{out})/L = [(5-2.8)V]/3\mu H = 0.733\ A/\mu s$.

From equation 1, the critical capacitance C_{crit} is given by:

$C_{crit} = 14\ A/[(0.733\ A/\mu s)(5\ m\Omega)] = 3.818\ mF$.

Since 10 mF is greater than 3.818 mF, C is greater than C_{crit} and thus R_o (as given by equation 5) is to be made equal to R_e. This is accomplished by compensating voltage error amplifier 59 as needed to obtain the transfer function of equation 4. When voltage error amplifier 59 is implemented as shown in FIG. 9, this compensation is achieved when the following two equations are satisfied:

$k*(R2/R1) = 1/(g*R_o)$ (Eq. 7)

$R_e*C = R2*C1$ (Eq. 8)

The value of g is determined by the transresistance of current sensor 64 and the implementation of current controller 66. If the first stage of the current controller is a voltage comparator (as here), g is equal to the reciprocal of the transresistance of current sensor 64. When the current sensor is implemented with a resistor, the transresistance is simply the resistor's resistance (thus, $g = 1/R_s$ in this example). In this example, equations 7 and 8 are satisfied when the following component values are used:

$R_1 = 1\ k\Omega$; $R_2 = 100\ k\Omega$; C1 = 500 pF. As the waveform of FIG. 10b shows, the output voltage response corresponds to a resistive output impedance of 5 mΩ, which is also equal to the ESR of the output capacitor.

An alternative implementation of feedback circuit 58 is shown in FIG. 11, in which voltage error amplifier 59 is implemented using a transconductance amplifier 90. A transconductance amplifier is characterized by an output current that is proportional to the voltage difference between its non-inverting and inverting inputs; the proportionality factor between the output current and the

input difference voltage is the amplifier's transconductance g_m. The voltage gain of a transconductance-type voltage error amplifier is equal to the product of the impedance connected to the output of transconductance amplifier 90 and the transconductance g_m.

The voltage error amplifier implementations shown in FIGs. 9 and 11 are equivalent when the following three equations are satisfied:

$g_m[(R_3R_4)/(R_3+R_4)] = R_2/R_1$ (Eq. 9)

$V_{ref}[R_4/(R_3+R_4)] = V_{ref}$ (Eq. 10)

$C_2[(R_3R_4)/(R_3+R_4)] = C_1R_2$ (Eq. 11)

Thus, the transfer function defined in equation 4 is obtained for voltage error amplifier 59 shown in FIG. 11 when each of equations 9, 10 and 11 are satisfied.

The invention is not limited to use with current-mode controlled voltage regulators that include a voltage error amplifier. One possible embodiment of the invention which uses neither current-mode control nor a voltage error amplifier is shown in FIG. 12. In this embodiment, a controllable power stage 100 produces an output voltage V_{out} in accordance with the voltage difference between a pair of inputs 102, 104; the power stage includes a power circuit 68 controlled by a fast voltage controller 105 which receives the inputs. In a switching voltage regulator, fast voltage controller 105 is characterized by rapidly increasing the duty ratio of the pulse train at its output when an appreciable positive voltage difference appears between inputs 102 and 104. In a linear voltage regulator, fast voltage controller 105 would typically be implemented with a wide-band operational amplifier.

The embodiment of FIG. 12 also includes a current sensor 106 having a transresistance R_s connected in series between the output of the power stage 100 and output node 52, which produces an output that varies with the regulator's output current. The current sensor's output is

connected to one input of a summing circuit 108, and a second summing circuit input is connected to output node 52. The summing circuit produces an output voltage equal to the sum of its inputs, which is connected to input 102 of power stage 100.

Input 104 of power stage 100 is connected to a node 110 located at the junction between a pair of impedances Z1 and Z2, which are connected in series between output node 52 and a voltage reference 112. When a regulator is configured as shown in FIG. 12, an optimal transient response is obtained by arranging the ratio between the two impedances Z2/Z1 in accordance with the following:

$$Z2/Z1 = [R_s(1+sR_eC)-R_s]/R_s \qquad \text{(Eq. 12)}$$

where R_s is defined by equations 5 and 6, R_s is the resistance of current sensor 106, and R_e and C are the ESR and capacitance of the output capacitor 56 employed.

One implementation of the voltage regulator embodiment of FIG. 12 is shown in FIG. 13. Fast voltage controller 105 is implemented with a hysteretic comparator 130, the output of which is connected to a driving circuit 132 which includes an upper driver 134 and a lower driver 136. Power circuit 68 includes an upper switch 138 and a lower switch 140, which are driven by drivers 134 and 136, respectively, and an output inductor L is connected to the junction between the switches. The hysteretic comparator 130 monitors the output voltage and turns off the upper switch when the output voltage exceeds the upper threshold of the comparator. The upper switch is turned on again when the output voltage drops below the comparator's lower threshold.

Current sensor 106 and summing circuit 108 are implemented with a series resistor 142 having a resistance R_3. Impedance Z1 is implemented with a parallel combination of a capacitor C_1 and a resistor R_4, and impedance Z2 is implemented with a resistor R_7.

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For the output impedance of the switching regulator of FIG. 13 to be equal to the resistance R_3, the ratio of the resistances of resistors R_6 and R_7 must be given by:

$R_7/R_6 = (R_3-R_z)/R_3$.

and the product of the capacitance of capacitor C_1 and the resistance of resistor R_6 must be given by:

$C_1R_6 = C[(R_0R_z)/R_3]$.

As is readily apparent to those skilled in the art of voltage regulator design, the voltage regulator embodiments and implementations discussed above are merely illustrative. Many other circuit configurations could be employed to achieve the invention's goals of optimum transient response and smallest possible output capacitor, as long as the inventive method is practiced as described herein.

The inventive method described herein can be presented as a general design procedure, applicable to the design of both linear and switching voltage regulators and accommodating the use of output capacitors having capacitances that are both greater than and less than the critical capacitance defined above. This design procedure can be practiced in accordance with the following steps:

1. Select a type of capacitor (such as Al electrolytic, ceramic, and OS-CON capacitors) to be used as the output capacitor for a voltage regulator required to maintain a regulated output voltage within a specified voltage deviation specification ΔV_{out} for a step change in load current ΔI_{load}.

2. Determine the characteristic time constant T_c for the selected capacitor type, which as explained above, is defined as the product of its ESR and its capacitance.

3. Determine the absolute value of the maximum available slope of the current injected by the voltage regulator toward the parallel combination of the output

load and output capacitor for a step increase in load current equal to ΔI_{load}, and the absolute value of the minimum available slope of the current injected toward the parallel combination of the output load and output capacitor for a step decrease in load current equal to ΔI_{load}. This is the done as described above in connection with equation 1.

4. Determine which of the two absolute values is smaller. The smaller absolute value is identified as m.

5. Determine a first capacitance C_0 in accordance with the following: $C_0 = [\Delta I_{load}^2/2m + mT_c^2/2]/\Delta V_{out}$.

6. Determine a resistance R_{e0} in accordance with the following: $R_{e0} = T_c/C_0$.

7. Determine a critical capacitance value C_{crit} in accordance with the following: $C_{crit} = \Delta I_{load}/mR_{e0}$.

8. If $C_0 < C_{crit}$, use an output capacitor having a capacitance C_1 about equal to C_0 and an equivalent series resistance R_{e1} about equal to R_{e0}.

If $C_0 \geq C_{crit}$, use an output capacitor having an equivalent series resistance R_{e2} about equal to $\Delta V_{out}/\Delta I_{load}$ and a capacitance C_2 about equal to T_c/R_{e0}.

9. Determine a resistance R_o in accordance with the following:

If $C_0 < C_{crit}$: $R_o = \Delta I_{load}/2mC_1 + [mC_1(R_{e1})]/2\Delta I_{load}$.

If $C_0 \geq C_{crit}$: $R_o = R_{e2}$.

10. Arrange the voltage regulator such that its output impedance, defined before its connection to the output capacitor used, is about equal to the series combination of resistance R_o and an inductance L_o, with L_o given by the following:

If $C_0 < C_{crit}$: $L_o = C_1 * R_{e1} * R_o$.

If $C_0 \geq C_{crit}$: $L_o = C_2 * R_{e2} * R_o$.

This step is accomplished by making the transfer function for the regulator's feedback circuit correspond with

equation 4, in accordance with the methods described above.

Note that time constant T_c (or its constituent factors C and R_e) is not a precisely defined quantity for a particular capacitor type. A number of factors, including manufacturing tolerances, case size, temperature and voltage rating, can all affect T_c. Thus, in a practical design, the parameter T_c used in the calculations should be considered as an approximate value, and a number of iterations through the design procedure may be necessary.

The inventive method can also be presented as a procedure specifically directed to the design of a buck-type switching voltage regulator employing current-mode control, which minimizes the size of the regulator's output capacitor while ensuring that its output voltage V_{out} is maintained within a specified voltage deviation specification ΔV_{out} for a step change in load current ΔI_{load}. This type of regulator has a pair of switches connected in series between an input voltage V_{in} and ground, with the junction between the switches connected to an output inductor. The switches are driven to alternately connect the inductor to V_{in} and to ground. Note that the design procedure below is applicable only for the case when $C > C_{crit}$, and as such it achieves the optimum load transient response shown in FIG. 6a; a buck-type regulator employing current-mode control could also use an output capacitor having a capacitance less than C_{crit} - and thereby achieve the optimum response shown in FIG. 7a - by following the design procedure described above. The design procedure applicable when $C > C_{crit}$ can be practiced by following the steps below:

1. Calculate a maximum equivalent series resistance $R_{e(max)}$ for the regulator's output capacitor in accordance with the following: $R_{e(max)} = \Delta V_{out}/\Delta I_{load}$.

2. Determine a minimum inductance L_{min} for the regulator's output inductor in accordance with the

following: $L_{min} = (V_{out}T_{off}R_{e(max)})/V_{ripple,p-p}$,
where T_{off} is the off time of the switch which connects the output inductor to V_{in}, and $V_{ripple,p-p}$ is the maximum allowable peak-to-peak output ripple voltage.

3. Use an output inductor with an inductance L1 which is equal to or greater than L_{min}.

4. Determine a minimum capacitance C_{min} for the output capacitor in accordance with the following:
if $V_{out} < (V_{in}-V_{out})$: $C_{min} = \Delta I_{load}/[R_{e(max)}(V_{out}/L1)]$;
if $V_{out} > V_{in}-V_{out}$: $C_{min} = \Delta I_{load}/[R_{e(max)}((V_{in}-V_{out})/L1)]$.

5. Use an output capacitor having a capacitance C about equal to C_{min} and an equivalent series resistance R_e about equal to $R_{e(max)}$.

6. Arrange the output impedance of the regulator to be about equal to R_e. This step is accomplished by making the transfer function for the regulator's feedback circuit correspond with equation 4, in accordance with the methods described above.

While particular embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. For example, a trivial alternate embodiment of a buck-type switching regulator has the second switch replaced with a rectifier diode. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

The invention is intended for use with voltage regulators for which output capacitor size and cost are preferably minimized, which must maintain its output voltage within specified boundaries for large bidirectional step changes in load current. These goals are achieved by employing an output capacitor that has a combination of the largest possible equivalent series resistance (ESR) and lowest possible capacitance that ensures that the peak-to-peak voltage deviation for a bidirectional step change in load current is no greater than the maximum allowed, and by compensating the regulator to ensure a response that is flat after the occurrence of the peak deviation - referred to herein as an "optimum response". When these conditions are met, the regulator's output capacitor will be the smallest possible capacitor which enables the output voltage to stay within the specified boundaries for a bidirectional step change in load current. The invention is applicable to both switching and linear voltage regulators.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

4. BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art switching voltage regulator circuit.

Fig.2 comprises a and b.

~~FIG. 2~~a and 2b are plots of output voltage and load current, respectively, for a prior art voltage regulator circuit which does not include a resistor connected between its output terminal and its output capacitor.

Fig.3 comprises a and b.

~~FIG. 3~~a and 3b are plots of output voltage and load current, respectively, for a prior art voltage regulator circuit which does include a resistor connected between its output terminal and its output capacitor.

3/4

Fig. 4 comprises a and b.

FIG. 4a and 4b are plots of output voltage and load current, respectively, for a prior art voltage regulator circuit in which the load current steps down before the output voltage has settled in response an upward load current step.

FIG. 5 comprises a ~ e.

FIG. 5a is a plot of a step change in load current,

FIG. 5b is a plot of the output current injected by a voltage regulator toward the parallel combination of output capacitor and output load in response to the step change in load current shown in FIG. 5a,

FIG. 5c is a plot of a voltage regulator's output capacitor current in response to the step change in load current shown in FIG. 5a,

FIG. 5d is a plot of a voltage regulator's output voltage when the capacitance of its output capacitor is greater than a critical capacitance C_{crit},

FIG. 5e is a plot of a voltage regulator's output voltage when the capacitance of its output capacitor is less than a critical capacitance C_{crit}.

Fig. 6 comprises a and b.

FIG. 6a and 6b are plots of output voltage and load current, respectively, for a voltage regulator per the present invention which employs an output capacitance that is equal to or greater than a critical capacitance C_{crit}.

Fig 7 comprises a and b.

FIG. 7a and 7b are plots of output voltage and load current, respectively, for a voltage regulator per the present invention which employs an output capacitance that is less than a critical capacitance C_{crit}.

FIG. 8 is a block/schematic diagram of an embodiment of a voltage regulator per the present invention.

FIG. 9 is a schematic diagram of one possible implementation of the voltage regulator embodiment shown in FIG. 8.

Fig 10 comprises a and b.

FIG. 10a and 10b are simulated plots of output voltage and load current, respectively, for a voltage regulator per FIG. 9.

FIG. 11 is a schematic diagram of alternative implementation of the voltage error amplifier shown in FIG. 9.

FIG. 12 is a block/schematic diagram of another embodiment of a voltage regulator per the present invention.

FIG. 13 is a schematic diagram of one possible implementation of the voltage regulator embodiment shown in FIG. 12.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a means of determining the smallest possible capacitor that can be used on the output of a voltage regulator in applications requiring large bidirectional step-like changes in load current, which enables the regulator's output voltage to remain within specified boundaries for a given step size. A given step change in load current is identified herein as ΔI_{load}, and the allowable output voltage deviation specification is identified as ΔV_{out}. As used herein, the "smallest possible output capacitor" refers to the output capacitor having the smallest possible capacitance value and the largest permissible ESR value which enable the regulator to meet the ΔV_{out} specification. Because the cost of a capacitor tends to be inversely proportional to its ESR and directly proportional to its capacitance, and because space is nearly always at a premium on a circuit board, the invention makes it possible for the output capacitor's cost and space requirements to be minimized.

The invention takes advantage of the realization that there is a smallest possible output capacitor that, when used with a properly configured voltage regulator, enables the regulator to meet a given ΔV_{out} specification. Neglecting the effect of the output capacitor's equivalent series inductance, a step change in load current ΔI_{load}

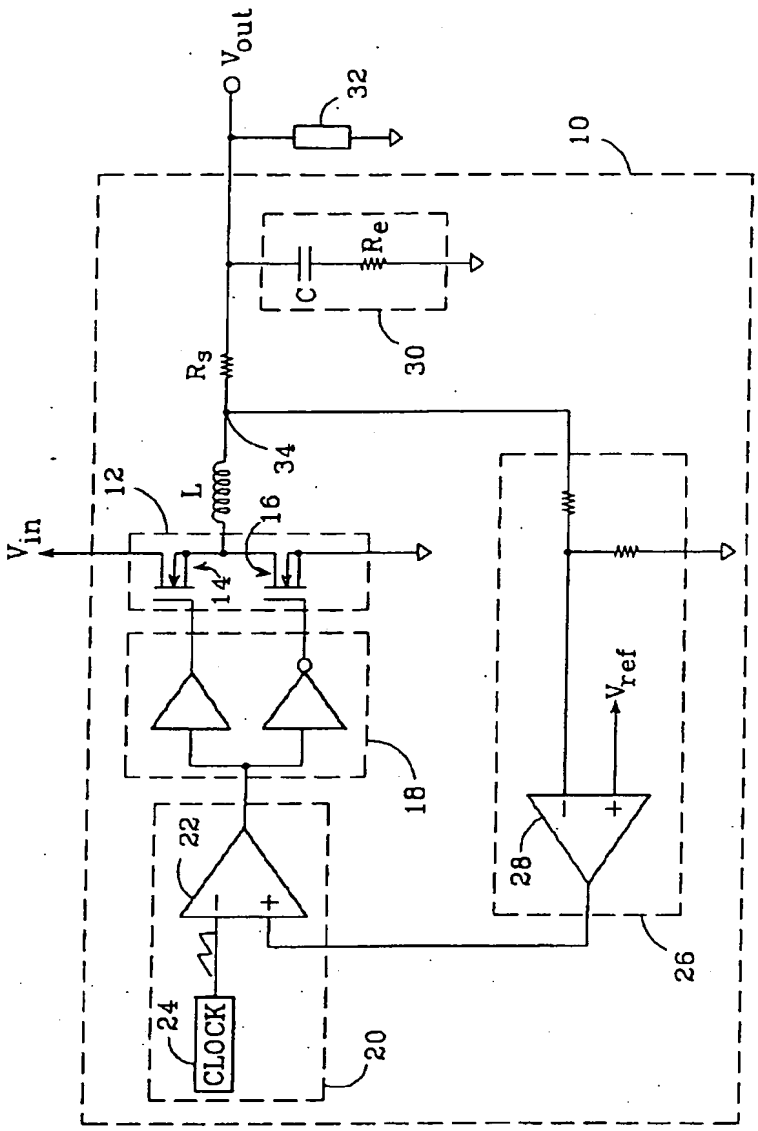

FIG. 1
(Prior Art)

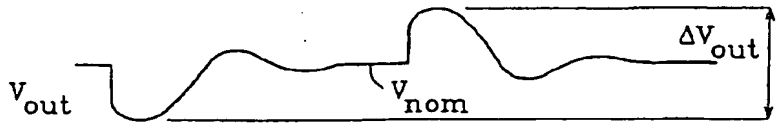

FIG.2a (Prior Art)

FIG.2b (Prior Art)

FIG.3a (Prior Art)

FIG.3b (Prior Art)

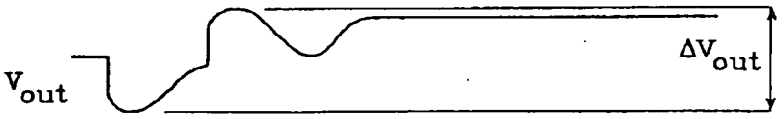

FIG.4a (Prior Art)

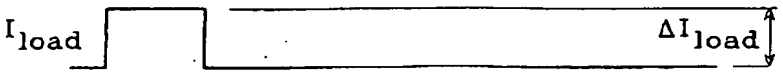

FIG.4b (Prior Art)

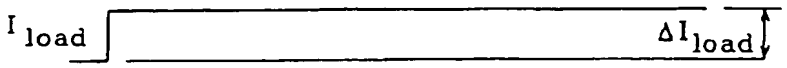

FIG.5a

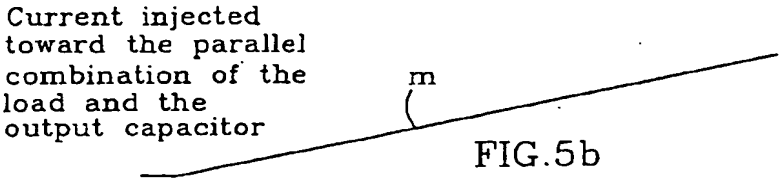

FIG.5b

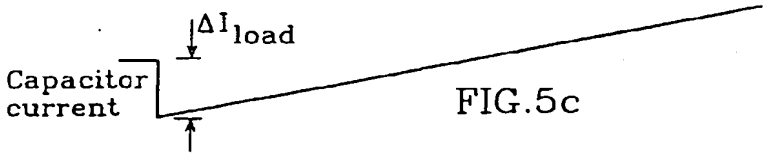

FIG.5c

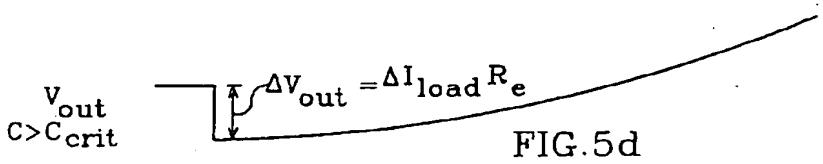

FIG.5d

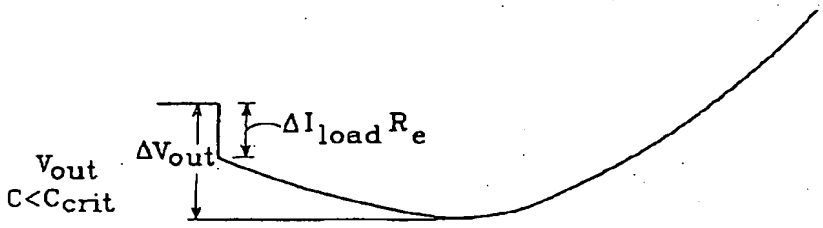

FIG.5e

FIG.6a

FIG.6b

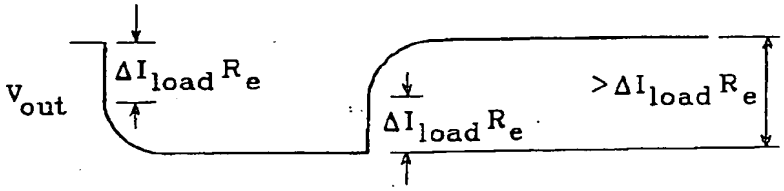

FIG.7a

FIG.7b

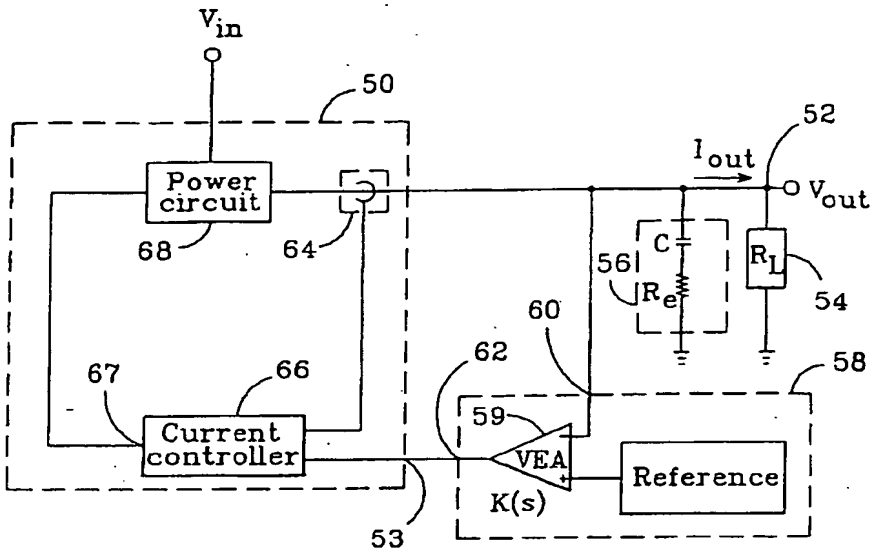
V_{in}
50
52
I_{out}
V_{out}
Power circuit
68
64
C
56
R_e
R_L
54
60
62
58
67
66
59
Current controller
VEA
Reference
K(s)
53

FIG.8

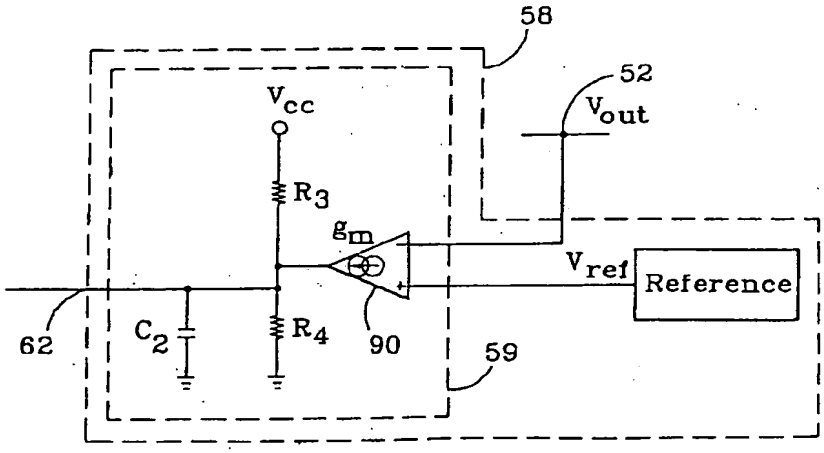
58
52
V_{cc}
V_{out}
R_3
g_m
V_{ref}
Reference
62
C_2
R_4
90
59

FIG.11

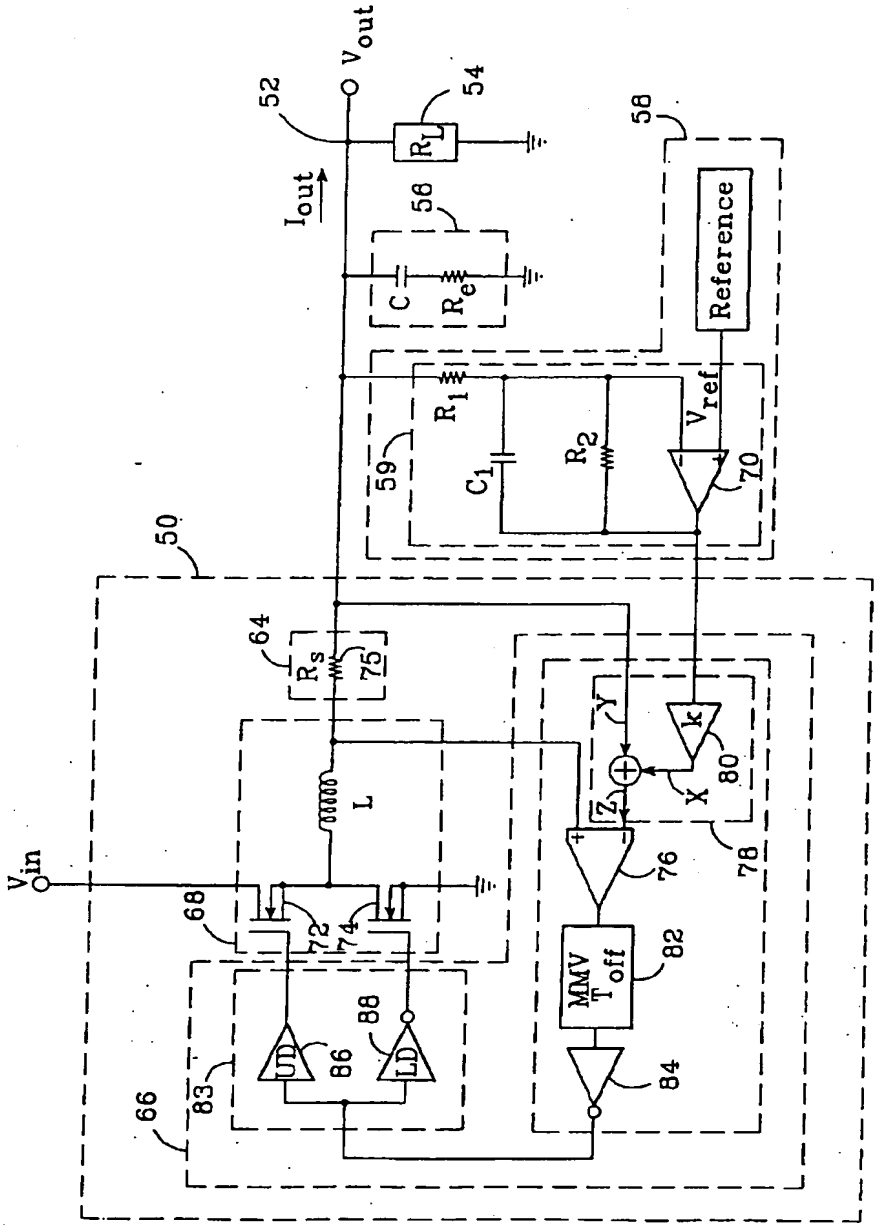
Vout
52
54
RL
Iout
56
C
Re
58
Reference
R1
C1
R2
Vref
59
70
50
64
Rs
75
Y
k
80
X
Z
76
78
L
Vin
68
72
74
MMV
Toff
82
88
UD
86
LD
84
66
83

FIG.9

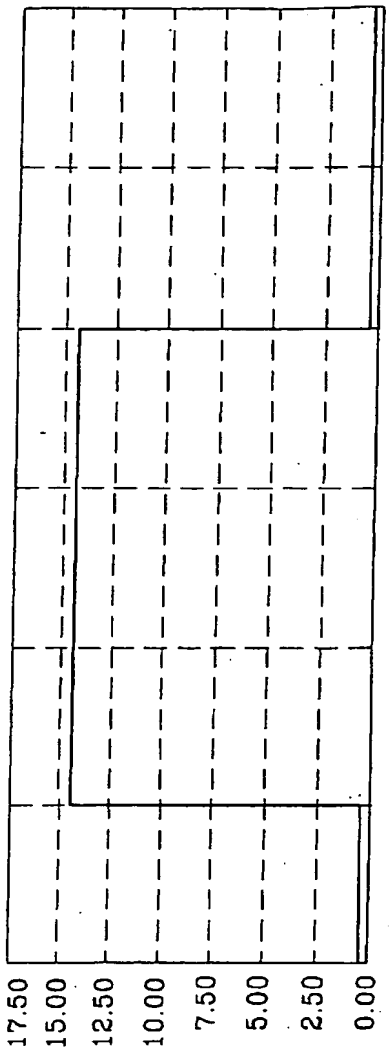

FIG.10a

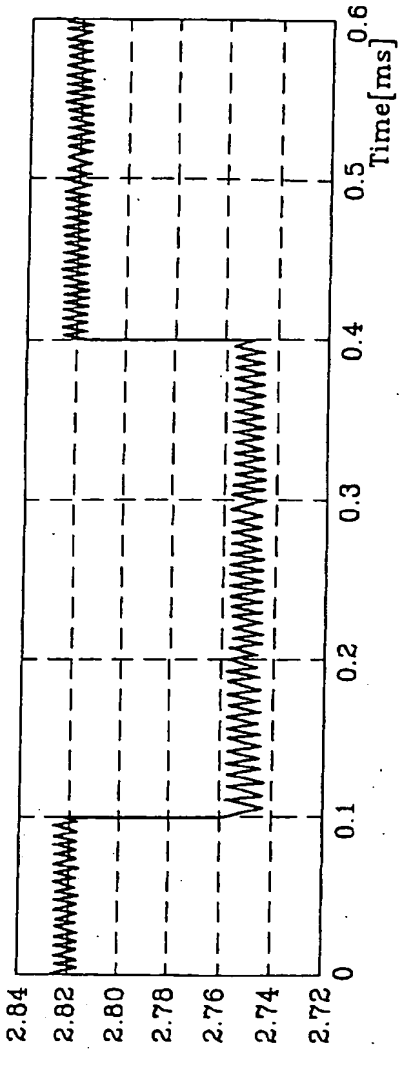

FIG.10b

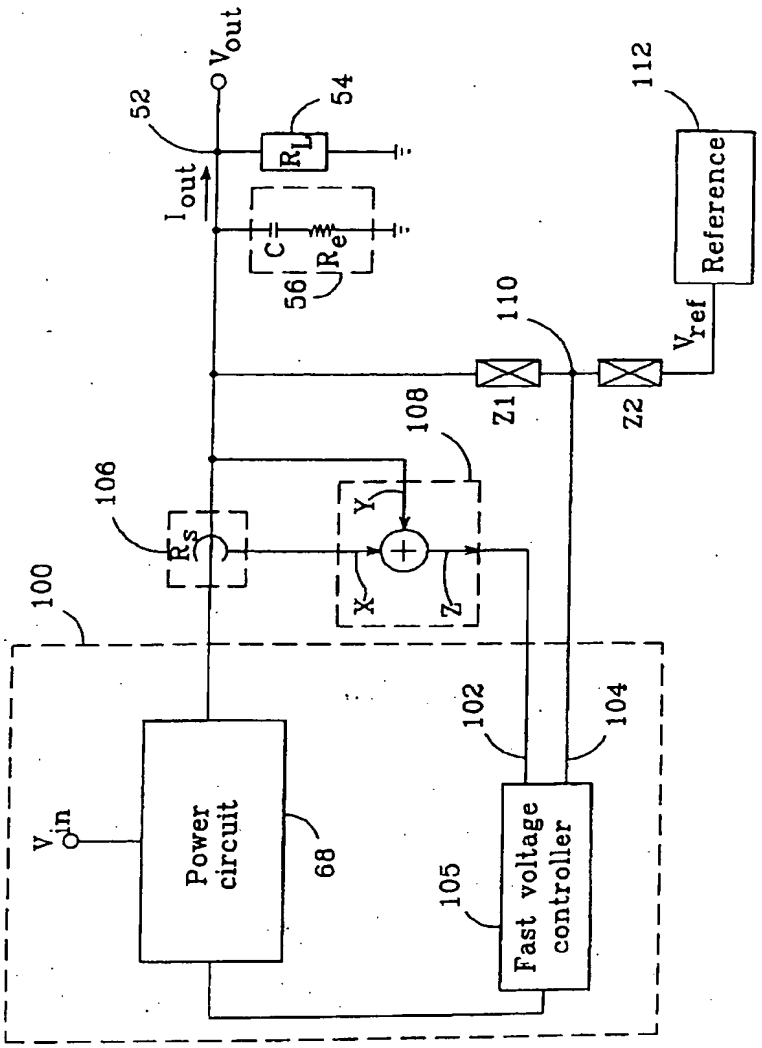
V_{out}
52
54
R_L
I_{out}
C
R_e
56
112
Reference
V_{ref}
110
Z1
Z2
108
106
R_s
Y
X
Z
100
102
104
V_{in}
Power circuit
68
105
Fast voltage controller

FIG.12

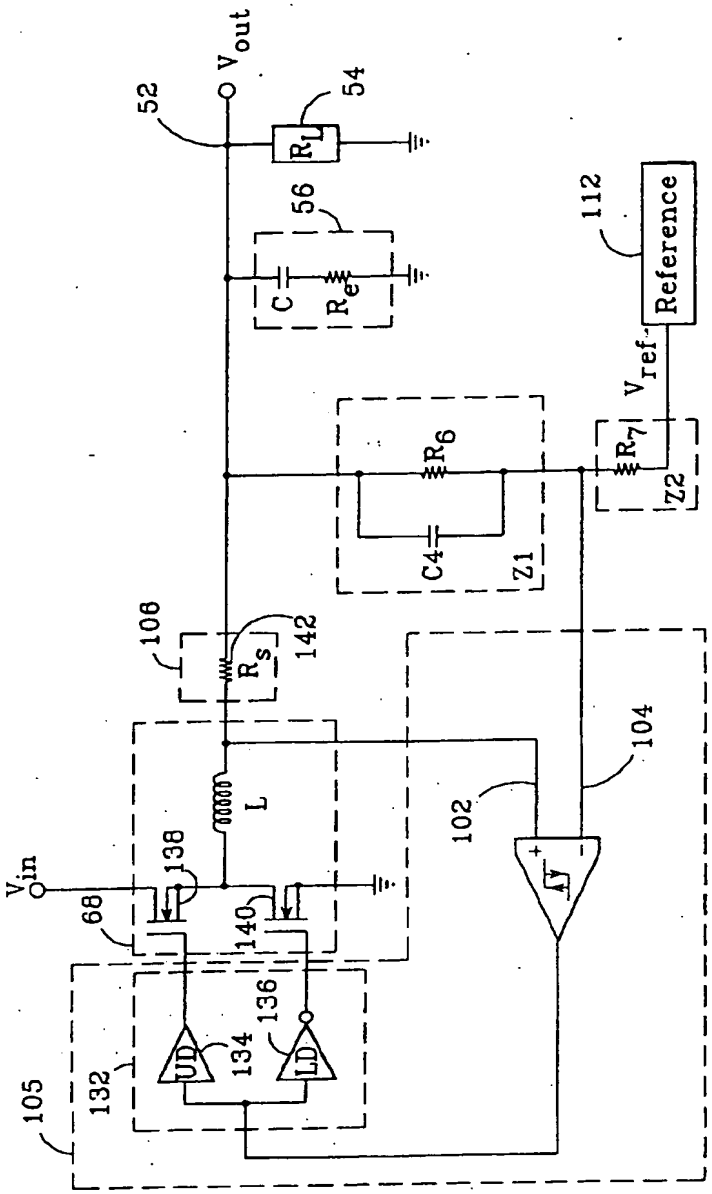
V_{out}
52
54
R_L
56
C
R_e
112
Reference
V_{ref}
R_6
R_7
Z2
C4
Z1
106
R_s
142
104
102
L
V_{in}
138
68
140
136
UD
134
LD
132
105

FIG.13

1. Abstract

A method and circuit enable a voltage regulator to employ the smallest possible output capacitor (56) that allows the regulator's output voltage (V_{out}) to be maintained within specified boundaries for large bidirectional step changes in load current. This is achieved by employing an output capacitor which has a combination of the largest possible equivalent series resistance (ESR) and lowest possible capacitance that ensures that the peak voltage deviation for a step change in load current (ΔI_{load}) is no greater than the maximum allowed (ΔV_{out}), and by compensating the regulator to ensure a response that is flat after the occurrence of the peak deviation. The invention is applicable to both switching and linear voltage regulators.

2. Representative Drawing

Fig. 8.

[JP,2000-299978,A]

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About the field of a voltage regulator, if this invention is specified further, it relates to the approach of improving the response of the voltage regulator to the transient of a load.
[0002]
[Description of the Prior Art] Even if the purpose of a voltage regulator is the case where a demand of the changed load current for which electric power is supplied to non-adjusted input voltage must be filled, it is supplying almost fixed output voltage to a load.
[0003] to sharp increase or reduction of the suddenly of the load current demanded by step status change-ization of the load current, i.e., a load, depending on an application, in order to maintain the output voltage of about 1 law, a regulator is needed. For example, when a microprocessor may have "power saving mode", turns OFF the circuit part which is not used in this case, reduces current consumption to zero mostly and is needed, it must set these parts to ON, and the load current must usually be raised to a high value within in hundreds of nanoseconds in that case.
[0004] If the load current has change, it is unescapable that a certain deflection arises in the output voltage of a regulator in practice. The magnitude of this deflection is related to both the capacity of an output capacitor, and equivalent series resistance (ESR). That is, deflection becomes large, so that ESR is so large that capacity is small. for example, in a switching voltage regulator (the output current is sent out through an output inductor and the output capacitor connected to juxtaposition between loads is included) Only Iload increases in [the current with which change (deltaIload) of the load current is sent out to one load] instant. Or the capacity of 2 output capacitor is very large, and since the ESR is still very smaller, if it is not extent which the deflection of output voltage can disregard, a result from which the output voltage of a regulator changes will be brought. The first alternative is impossible. It is because the current in an output inductor cannot change in an instant. Although time amount required in order to cope with change of the load current can be shortened by making the inductance of an output inductor small, for that, the rise of the switching frequency of a regulator is needed after all, and it is restricted by the dissipation in the limited switching rate of a switching transistor, and the drive circuit of a transistor. Although the 2nd alternative is possible, possibility of a very big output capacitor being needed, the space occupied on a printed circuit board being too large to remainder, or cost starting too much, or becoming these both sides is high.
[0005] For the application with which the specification which restricts the deflection of permissible output voltage for the output voltage of a regulator narrowly to a narrow load transient response specification, i.e., a bidirectional step change of the load current, must be filled, it may become so large that this unescapable deflection cannot be admitted. When using here, "deltaVout" shall mean the peak pair peaking capacity voltage deviation shown in a graph

while meaning the output voltage deflection specification of a regulator. The clearest solutions for improving a load transient response are increase of an output capacitance, and/or reduction of ESR of an output capacitor. However, a cost rise is caused, in order that the required volume (volume) may become large and may make PC-board area large so that an output capacitor becomes large (capacity becomes large and ESR becomes small) as described previously.
[0006] One of the technique which improves a load transient response is shown in drawing 1 . The switching voltage regulator 10 contains the push and pull switch 12 connected between supply voltage Vin and touch-down. Two power metal-oxide semiconductor field effect transistor 14 and 16 changed synchronous usually realizes this. A driver circuit 18 is connected and one side or another side of MOSFETs 14 and 16 is changed by turns. The duty ratio modulation circuit 20 controls a drive circuit. A circuit 20 contains the electrical-potential-difference comparator 22 which compares the error voltage received from the saw-tooth-wave clock signal received from the clock circuit 24, and the error signal generating circuit 26. Usually, including the high interest profit operational amplifier 28, a circuit 26 receives the electrical-potential-difference expression of output voltage Vout in reference voltage Vref and the 2nd input in one input, and generates the error voltage changed with the difference of Vout and desired output voltage. Moreover, a regulator contains the resistor RS connected between the output capacitor 30 shown by expressing as the output inductor L connected to the join between MOSFETs 14 and 16, equivalent series resistance Re, and an in-series capacity C, the output inductor, and the output capacitor. Vout is connected and a load 32 is driven.
[0007] In actuation, MOSFETs 14 and 16 are driven so that Inductor L may be connected to Vin and touch-down by turns, and a duty ratio is determined by the duty ratio modulation circuit 20. A duty ratio is changed according to the error voltage which the error amplifier 28 generates. The current of Inductor L flows into the parallel connection of the output capacitor 30 and a load 32. On a switching frequency, since the impedance of a capacitor 30 is farther [than that of a load 32] small, a capacitor filters most AC components of an inductor current, it removes, and all the direct currents are sent out to a load 32 as a matter of fact.
[0008] If there is no series resistance machine RS, the electrical potential difference fed back to a circuit 26 will become equal to Vout, and the response to the step change in the load current of a regulator will serve as it of a typical switching regulator. The output voltage Vout of the regulator to step change of the load current Iload shown in drawing 2 b is shown in drawing 2 a. Since it cannot change in an instant, if Iload changes suddenly, Vout will fall in the shape of a spike, and, finally, as for the current of L, a control loop will pull back Vout on the nominal-output electrical potential difference Vnom. Similarly, when Iload falls in the shape of a step after that, Vout goes up in the shape of a spike, and returns to Vnom after that. The total deflection in output voltage deltaVout to step change of the load current is determined by the difference between two peaks of an electrical-potential-difference spike. When the regulator is restrained by the narrow load transient response specification, this deflection may exceed the tolerance allowed.
[0009] connecting Resistance RS to Inductor L and a serial -- (-- an output terminal 34 -- setting --) -- deltaVout can be decreased. To step change of the load current shown in drawing 3 b, when RS is included, one of the possible responses is shown in drawing 3 a. When RS is contained in a proper place, a control loop does not already restore Vout to Vnom, and restores Vout to the electrical potential difference given with the value which subtracted the product of deltaIload and RS from the electrical potential difference in a terminal 34 rather. That is, only delta load*RS becomes high rather than the case where the steady state value of Vout to a light load receives a

heavy load. By making RS almost equal to ESR of an output capacitor, some narrow deltaVout(s) can be obtained rather than it is obtained, when not using RS.
[0010] About the fault of the circuit of drawing 1 , one of them is shown in drawing 4 a and drawing 4 b. In this case, the load current (drawing 4 b) falls in the shape of a step again, before Vout (drawing 4 a) stabilizes in a steady state value. If high rather than Vout can set to drawing 3 a when Iload falls, the peak of a upward Vout spike will also become high and overall deflection deltaVout will become larger than the case of being other. Thus, in order for that deflection becomes large to fulfill a narrow output voltage deflection specification especially, a regulator 10 must use a bigger output capacitor and the ESR means becoming small-like proportionally. Since the cost of a capacitor is in inverse proportion to that ESR in approximation, as for costs, it may start [fulfilling this specification] too much.
[0011] Another fault of the circuit of drawing 1 is that remarkable power consumption is needed for the series resistance machine RS. For example, if RS is assumed to be 5mohm and a maximum load current is assumed to be 14.6A, the consumption in RS will be set to 1.07W.
[0012] In improving the load transient response of a regulator, the technique using a different control principle D. "V2 of Goder (D. GODA) and W.R.Pelletier (W. R. PERECHIA) Architecture Provides Ultra?Fast Transient Response in Switch Mode Power Supplies" (V2 architecture brings about a ultra high-speed transient response in a switch-mode power supply), HFPC It is indicated by Proceedings and 19 - 23 pages in PowerConversion and September, 1996. The regulator indicated in this contains an output inductor and a capacitor same with having been shown in a push and pull switch, a driver circuit, an error amplifier, and drawing 1 . The signal showing the output voltage of a regulator is supplied to both error amplifier and an electrical-potential-difference comparator. An electrical-potential-difference comparator also receives the output of error amplifier. When the output voltage of a regulator exceeds the output of an error amplifier, the output of a comparator shifts to quantity, carries out the trigger of the monostable multivibrator, and turns OFF an upper switching transistor covering a predetermined time interval.
[0013] The transient response of this circuit is designed so that it may become more nearly high-speed than that of the circuit of drawing 1 . The step of the load current changes the electrical potential difference in a comparator immediately, bypasses blunt error amplifier, and shortens the response time by this. However, even if the response time becomes short, the configuration of response trace can be similar with what is still shown in drawing 3 a, and any improvement cannot almost be found in the magnitude of deltaVout.
[0014] Another switching regulator is "Fueling of L.Spaziani (L. SUPATCHIANI). the Megaprocessor ? DC/DC Converter Design Review Featuring the UC3886 and UC3910" (examination of the DC/DC converter design characterized by electric supply ?UC3886 of a megger processor, and UC3910), Unitrode Application Note It is indicated by U?157, 3?541, or 3?570 pages. The control principle which adjusts by controlling the average of the current in an output inductor and which is known as "average current control" is used for this regulator. A resistor is connected to the output inductor of a regulator, and a serial, current detection amplifier (CSE:current sense amplifier) is connected between this resistor, and an inductor current is detected. The output of CSE is supplied to current error amplifier with the output of electrical-potential-difference error amplifier. Electrical-potential-difference error amplifier compares the output voltage of a regulator with reference voltage. A comparator receives a saw-tooth-wave clock signal in the output of current error amplifier, and the input of another side in one input. A

comparator generates a pulse-width-modulation output and drives a push and pull switch through a driver circuit.
[0015] In actuation, according to increase of the load current, output voltage decreases and the error signal from electrical-potential-difference error amplifier increases. For this reason, the duty ratio of the pulse which the output from a current error amplifier increases, therefore a comparator generates becomes large. Then, the current in an output inductor increases and output voltage is pushed up. Electrical-potential-difference error amplifier is constituted so that non-storage gain may be given, and this is combination with average current control, and gives limited and controllable output resistance to a regulator. Thereby, positioning of output voltage becomes being the same as that of the mode to which the series resistance machine RS affects the response of the circuit of drawing 1 . However, the response obtained is similar to it of drawing 3 a also in this case, and deltaVout may still exceed a narrow output voltage deflection specification as clearly shown in drawing 32 of bibliography.
[0016]
[Problem(s) to be Solved by the Invention] The problem described previously is conquered, and the approach and circuit where a voltage regulator can obtain the optimal response to a big bidirectional load transient are offered, using the minimum output capacitor as much as possible.
[0017]
[Means for Solving the Problem] As for this invention, it is desirable to hold down the size and cost of an output capacitor to min, and it means using with the voltage regulator which must maintain the output voltage within the boundary specified to a big bidirectional step change of the load current. A regulator is compensated so that the response which becomes flat may be secured after generating of the peak deflection which adopts the output capacitor which has the combination of the equivalent series resistance (ESR) greatest as much as possible and the capacity minimum as much as possible, and is called "the minimum response" here with which it compensates that the peak pair peak voltage deflection to the bidirectional step change in the load current is below permission maximum in attaining these targets. If these conditions are fulfilled, the output capacitor of a regulator will turn into the minimum capacitor for which it makes it possible to stop output voltage within the boundary specified to the bidirectional step change in the load current as much as possible. This invention is applicable to both switching and a linearity voltage regulator.
[0018] Still more nearly another description and advantage of this invention will become clear to this contractor by referring to the following detailed explanation with an accompanying drawing.
[0019]
[Embodiment of the Invention] This invention provides the output of a voltage regulator with a means to determine the usable capacitor minimum as much as possible, in the application which needs big bidirectional step status change-ization for the load current. Thereby, the output voltage of a regulator becomes possible [maintaining within the boundary specified to given step size]. Here, the given step change in the load current is identified as deltaIload, and a permissible output voltage deflection specification is identified as deltaVout. When using here, "the output capacitor minimum as much as possible" shall mean the thing of an output capacitor which has the capacity value minimum as much as possible and the greatest ESR value minimum as much as possible which may be allowed which enables a regulator to fulfill deltaVout specification. Since the cost of a capacitor tends to be proportional to the capacity directly in inverse proportion to the ESR, and since space is almost always precious on a circuit board, this

invention makes it possible to minimize the cost and the requirements for space for an output capacitor.

[0020] This invention will use the reality which enables a regulator to fulfill given deltaVout specification in which there is the minimum output capacitor as much as possible, if the voltage regulator constituted proper is used. When the effectiveness of the equivalence serial inductance of an output capacitor is disregarded, step change deltaIload of the load current makes the output voltage of a voltage regulator generate initial change. This is equal to ESR (here, it identifies as Re) of a capacitor and the product of deltaIload, i.e., Re*delta Iload. This initial change is produced to a load current step above and down [both]. When it is beyond the "critical (critical)" value Ccrit with the capacity C of an output capacitor (it discusses in detail below), output voltage deflection cannot exceed an early Re*delta Iload change. When C is under Ccrit, output voltage deflection continues increasing, before beginning to restore after that after early Re*delta Iload changes.

[0021] The regulator of the conventional technique is usually designed so that output voltage may be again driven toward nominal value after transient generating of a load. However, if it does in this way, overall output voltage deflection deltaVout may reach even the twice of Re*delta Iload. If the load current goes up in the shape of a step, as for Vout, only Re*delta Iload will fall from nominal voltage. When the load current has stopped at quantity sufficiently long, as for a regulator, Vout is again driven to nominal voltage. Here, if the load current falls in the shape of a step again, as for Vout, only Re*delta Iload will go up in the shape of a spike, and, as a result, full power voltage deviation will be set to 2 (Re*delta Iload).

[0022] I hear that the response that whose the fault which is inherent in the control approach for the magnitude of deltaVout of the regulator of the conventional technique has been recognized, and was found generates the optimal load transient response, i.e., the minimum output voltage deflection deltaVout, is a response which stops at the voltage deviation boundary by the side of Gokami of a downward load current step uniformly, and stops at it uniformly on the voltage deviation boundary of the back bottom of a upward load current step, and there was. This invention offers the approach of constituting a regulator so that the load transient response of a regulator may serve as this theoretical optimum value or its near. Moreover, it turned out that it is the minimum capacitor which can be used in order that an output capacitor required in order to attain this response may fulfill the specification of deltaVout as much as possible.

[0023] The target to obtain the optimal response is attained, and many steps must be performed in order to specify the minimum capacitor which makes possible given deltaVout specification which should be fulfilled by this as much as possible. The maximum equivalent series resistance Re (max) is determined to the output capacitor which the voltage regulator which first receives constraint of voltage deviation assignment deltaVout specified to bidirectional step change deltaIload of the load current adopts. According to Ohm's law, Re (max) is given by Re(max) =delta Vout/delta Iload. When Re of an output capacitor is as larger as possible than Re (max), the initial deviation of Vout to step change of the load current equal to deltaIload surely exceeds deltaVout.

[0024] The following step is determining the above-mentioned "critical" capacity value Ccrit. It be the thing of the amount of the capacity which make the inclination of output voltage zero in case it go up to the letter of an inclination with the inclination of the max allow the current pour in by the regulator toward the parallel connection of a load and output capacitor when it connect at juxtaposition between the loads which drive critical capacity by the voltage regulator (as the output capacitor of a regulator) by physical limit of a regulator (or descent) , namely , make flat

after an early Re*delta Iload change . The thing of the greatest inclination allowed by physical limit of a regulator is made to call it "the inclination for maximum good (maximum available slope)" here.--

[0025] The critical capacity Ccrit is given by the following formula.

[0026]

[Equation 11]

Ccrit=delta Iload/mRe (max) (formula 2)

Here, deltaIload is an inclination value relevant to the current which turned the maximum anticipation load current step and Re (max) to the maximum-permissible output capacitor ESR (it calculated previously), turned m to the parallel connection of an output capacitor and an output load, and was poured in, and discusses below the approach of determining m and its value.

[0027] The inclination parameter m is shown in drawing 5 a thru/or drawing 5 c. Drawing 5 a shows the load current wave over an above step. Drawing 5 b shows the current which the regulator poured in towards an output capacitance when a regulator generates the output current in the inclination m for maximum good, and the parallel connection of an output load. Drawing 5 c shows the current in an output capacitor, and this current is equal to the difference of the load current and an inrush current.

[0028] When the capacity of regulator ** is larger than Ccrit (drawing 5 d), and when smaller than Ccrit (drawing 5 e), as for drawing 5 d and drawing 5 e, the size of the output capacitor of a regulator affects Vout how, and a regulator shows pouring in a current with the inclination for maximum good towards the parallel connection of a capacitor and a load. In C>Ccrit, it is begun to restore Vout immediately after generating of initial deltaIloadRe change. However, in C<Ccrit, after initial deltaIloadRe change continues increasing and, finally, the deflection of output voltage is restored after that.

[0029] The inclination value m over a given regulator is influenced by the configuration. Generally, m is decided as follows.

1) Determine the absolute value of the inclination for maximum good of the current which a voltage regulator pours in towards the parallel connection of an output load and an output capacitor to the increment in a step of the load current equal to deltaIload.

2) Determine the absolute value of the inclination for minimum good of the current poured in towards the parallel connection of an output load and an output capacitor to step reduction of the load current equal to deltaIload. An inrush current will have negative inclination as a result of the step-like reduction in the load current. As opposed to step-like reduction in [as opposed to / next / this step] "load current ... Inclination" for maximum good becomes equal to the greatest negative inclination.

3) Judge the which one is small between two absolute values. This is the inclination for maximum good of the "worst situation." The smaller one serves as a value m between two absolute values, and it is used in the formula for which it asked here.

[0030] The inclination m for maximum good of the worst situation is clearly defined in a switching regulator by the input voltage Vin, its output voltage Vout, and the inductance L of the output inductor. For example, in a back mold voltage regulator (buck?type voltage regulator), m can be decided as follows. When Vout is under Vin-Vout, m is given by m=Vout/L. When Vout is larger than Vin-Vout, m is given by m=(Vin-Vout)/L.

[0031] The inclination for worst situation maximum good is not so defined clearly by the linearity voltage regulator. This is dependent on many factors which also include the value of the

load current as compensation of the electrical-potential-difference error amplifier, the physical characteristic of the semiconductor device, and possibility.
[0032] Two optimal load transient responses which can be attained by this invention are shown in drawing 6 and drawing 7 . Drawing 6 a shows the optimal load transient response to the bidirectional step in the load current shown in drawing 6 b about the regulator constituted proper, when the capacity C of an output capacitor is more than Ccrit. Since C is more than Ccrit, maximum output voltage deviation is restricted to Re*delta Iload. Drawing 7 a shows the optimal load transient response to bidirectional step change deltaIload in the load current of drawing 7 b, when the capacity of the output capacitor of the regulator constituted proper is under Ccrit. After the initial step (= Re*delta Iload) produced by Re of a capacitor, Vout inclines toward a steady state value gradually, and subsequently to, it stops uniformly in a steady state value until the load current falls in the shape of a step and returns. It can be shown that peak voltage deflection deltaVout in this case is given by the following formula.

[0033]
[Equation 12]
delta Vout=delta Iload2 / 2 mC+mCRe 2/2 (formula 2)
m and deltaIload are the same also in a formula 1 here, and C and Re are the capacity and ESR of the output capacitor to be used, respectively. The approach of guaranteeing it not exceeding the peak voltage deflection given by the formula 2 still more even if this invention is the case where the capacitor which has the capacity of under Ccrit must be used is offered. Therefore, when using here, as shown in drawing 6 a, a regulator answers the load current step of size deltaIload, and "the optimum response (optimum response) of initial output voltage deflection" to the regulator which has the output capacitor of a bigger capacity than Ccrit is equal to deltaIload*Re, and stops uniformly to the following load current step. When the capacity of an output capacitor is under Ccrit, an optimum response comes to be shown in drawing 7 a, and peaking capacity voltage deviation is given by the formula 2, and stops uniformly to the following load current step.
[0034] Once it determines the value of m to a given regulator, the capacitor (based on drawing 6 a or drawing 7 a) of the minimum size by which an optimum response is obtained can be determined. The capacitor of the minimum size is the capacity C and ESR with which are satisfied of the following formulas. It has the combination of Re.
[0035]
[Equation 13]
Cmin=[deltaIload2 / 2 m+mTC2/2]/deltaVout (formula 3)
Here, the inclination value which calculated m previously, the maximum allowable-voltage deflection to step change of the load current with deltaVout equal to deltaIload, and TC are property time constants (it discusses below).
[0036] The minimum size with which are satisfied of a formula 3 exists to the class of given capacitor. For example, (Aluminum aluminum) electrolyte capacitor, a ceramic condenser, and an OS-CON (aluminum which has organic-semiconductor electrolyte) capacitor are contained in the class of capacitor. Selection of the class of output capacitor is influenced according to many factors. In a switching regulator, one of the important points taking into consideration is a switching frequency. There is an inclination which uses aluminum electrolyte capacitor in the design (for example, 200kHz) of low frequency, by intermediate frequency design (for example,

500kHz), there is an inclination which uses an OS?CON capacitor and there is an inclination which uses a ceramic condenser by high frequency design (1MHz or more).
[0037] Once it chooses the class of capacitor, the property time constant TC will be determined. This is given by the product of the ESR and its capacity. Since ESR of a capacitor will tend to decrease if the capacity increases, TC tends to become almost fixed to the capacitor of a given class and a voltage rating. For example, a standard low-battery (for example, 10V) aluminum electrolyte capacitor has a property time constant for about 40 microseconds (for example, 2mFx20mohm), a ceramic condenser has a property time constant for about 100ns (for example, 10microFx10mohm), and an OS-CON capacitor has a property time constant for about 4 microseconds (for example, 100microFx40mohm).
[0038] According to a formula 3, the minimum capacity is decided using TC determined to the class of selected capacitor. Min ESR Re (max) is given by the following formula.
[0039]
[Equation 14] It is small ESR somewhat from this preferably [it is equal to the desirable larger capacity C and Re (max) equal to Re(max) =TC/CminCmin or than this, or]. The capacitor which has RC is used as an output capacitor of a regulator. In beyond the Ccrit value which C calculated previously, the response by drawing 6 a is obtained. When C is under Ccrit, a response like drawing 7 a is attained. Using the output capacitor which has ESR equal to capacity and Re (max) equal to Cmin does not recommend, although it is permissible. If it carries out like this, it will become a practically childish design and the safety margin to tolerance, secular change, temperature, etc. will not be obtained. Choosing the capacitor which, on the other hand, has ESR quite smaller than Re (max) does not recommend, either. It is because a capacitor tends to serve as cost quantity so that ESR is small. Once it decides the ESR value of an output capacitor, it will comment on the capacity C being mostly determined by selection of the class of capacitor. Therefore, although C may become quite larger than Ccrit, within the limits of the selected capacitor class, the size of a capacitor is still in the minimum state.
[0040] After choosing an output capacitor, it is necessary to constitute a voltage regulator so that the response may have the optimal configuration shown in drawing 5 a (when it is C>Ccrit) or drawing 6 a (when it is C<Ccrit). In order to attain an optimum response in C>Ccrit, a voltage regulator is constituted so that the output impedance (the impedance of an output capacitor is included) of a voltage regulator may serve as resistance and may become equal to ESR of an output capacitor. In C<Ccrit, an optimum response is the inclination for maximum good at association of a load and an output capacitor, and it is guaranteed only by making a current pour into a regulator until it reaches peak deflection. In this case, since a regulator operates in the nonlinear mode to the part of this response, it is unchanging to selection of an output impedance being possible so that the optimal output impedance cannot be defined or the almost optimal response may be obtained.
[0041] One operation gestalt of the voltage regulator by this invention is shown in drawing 8 . The good control power stage 50 answers the control signal received in a characterization eclipse and a control input 53 by Transconductance g, and generates an output Vout to the output node 52. The power stage 50 drives a load 54. It connects with juxtaposition between loads, and the output capacitor 56 is divided and shown in the capacitive component C and an equivalent-series-resistance Re component here. The feedback circuit 58 is connected between the output node 52 and the control input 53.
[0042] The electrical-potential-difference error amplifier 59 can be included, and the signal with which output voltage Vout is expressed in the 1st input 60 is connected so that reference voltage

may be received in the 2nd input, and a feedback circuit 58 generates the output 62 changed with the difference electrical potential difference during the input. With the operation gestalt shown in drawing 8 , when the optimal load transient response 56, i.e., a capacitor, is more than Ccrit and the optimal load transient response by drawing 6 a and a capacitor 56 are under Ccrit(s), the optimal load transient response by drawing 7 a is attained by compensating the electrical-potential-difference error amplifier 59 so that gain K (s) may be given by the following formula.
[0043]
[Equation 15]
K(s) =- (1/gR0) (1/(1+sReC)) (formula 4)
Here, g is the transconductance of the good control power stage 50, C and Re are the capacity and ESR of the output capacitor 56, respectively, and it is the amount to which s is given to with complex frequency and R0 is given by the following formula.
[0044]
[Equation 16]
In C>=Ccrit, it is R0=Re. (formula 5)
[0045]
[Equation 17]
In C<Ccrit, it is R0=(deltaIload/2mC)+ (mCRe2/2deltaIload).
(Formula 6)
Here, C and Re are the capacity and ESR of the output capacitor 56, respectively, m is the absolute value (it is as having discussed about the decision of Ccrit) of the liminal gradient of the current poured in towards the parallel connection of the output capacitor 56 and a load 54, and deltaIload is the maximum load current step designed so that a regulator might cope with it.
[0046] The value of R0 defined in the formula 5 and the formula 6 serves as a scale of the peak voltage deflection of a regulator. When C is more than Ccrit, it came to have defined gain [of the electrical-potential-difference error amplifier 59] K (s) as a formula 4, and the joint output impedance of a regulator and the output capacitor 56 becomes equal to the equivalent series resistance Re of an output capacitor. Therefore, peak voltage deflection serves as deltaIload*R0, and, in C>=Ccrit, this is equal to deltaIload*Re.
[0047] C was under Ccrit, and when it is as gain [of the electrical-potential-difference error amplifier 59] K (s) having defined it as the formula 4, it came to have defined peak voltage deflection deltaVout as a formula 2. When C is under Ccrit, a system cannot become nonlinear, therefore a regulator cannot attain the optimum transient response shown in drawing 6 a. However, if the transfer function which compensates the electrical-potential-difference error amplifier 59, and is given by the formula 4 is formed, the transient response in practice possible nearest to the ideal response of drawing 6 a will be obtained.
[0048] The good control power stage 50 is limited to neither of the specific configurations. The power stage 50 is constituted so that power modal control may be performed, and a power stage has transformer resistance equal to RS, and includes reception and the power circuit 68 which answers and generates output voltage Vout in drawing 8 for the output 67 from the current controller which generates reception and an output 67 for the output of the current sensor which generates the output signal changed with the output current of a power stage, and a current sensor, and the output 62 of electrical-potential-difference error amplifier as an input, and a current controller. This invention is applicable to both a linearity regulator and a switching regulator. In a linearity regulator, a power circuit 68 is a serial pass transistor, and the current controller 66 is amplifier. In a switching regulator, either of much topology containing a control

mold switch, diode, an inductor, a transformer, and a component part like a capacitor can have a power circuit 68. For example, the typical power circuit of a back mold switching regulator is shown in drawing 1. This contains the output inductor L connected among one pair of joints of the control switches 14 and 16-ed and a switch, and the output of a regulator.
[0049] For the current controller 66 of a switching regulator, two formats are possible. That is, they are an instant mold and an average mold. Instantaneous-carrying-current control For example, A.S.Kislovski (A. S. kiss lob clearance), R. Redl (R. REDORU) and N.O.Sokal (N. O. SOKARU), Dynamic analysis of switching?mode DC/DC converters (dynamic analysis of a switching mode DC/DC converter), Van Nostrand As indicated by Reinhold (1991) and 102 pages It has at least six kinds of different low order formats. Fixed off time amount peak current control, Fixed ON time amount ballet current control, hysteria tick control (hysteretic control), constant frequency peak current control, constant frequency ballet current control, and PWM conductance control are included. Although an instantaneous-carrying-current controller can change the current in an output inductor within a 1 switching period, it usually requires for several terms to change an inductor current by average current control. Although the instantaneous-carrying-current control is more desirable because of this reason, an average current controller has the response with a current control loop quick enough, and it is usable in order to realize this invention. However, this embodiment has the fault of needing current error amplifier, and causes the complexity of a regulator circuit, and the rise of cost.
[0050] Drawing 9 is the schematic diagram of 1 possible operation gestalt of the switching voltage regulator by this invention. As for the electrical-potential-difference error amplifier 59, the feedback circuit 58 is constituted from this operation gestalt by the operational amplifier 70, the input resistor R1, the feedback resistor R2, and the feedback capacitor C1 including the electrical-potential-difference error amplifier 59. The joint during these switches is connected to the output inductor L including one pair of switches 72 and 74 to which the power circuit 68 was connected between Vin and touch-down. The resistor 75 which has Resistance RS realizes and the current sensor 64 is connected to the serial between Inductor L and the output node 52.
[0051] The current controller 66 is a fixed off time amount peak current control mold controller, and contains the electrical-potential-difference comparator 76. The input of the electrical-potential-difference comparator 76 is connected to the output of the inductor side of a resistor 75, and an adder circuit 78. An adder circuit 78 generates an electrical potential difference equal to the output Z to the sum of the electrical potential difference of the X and Y input. X is connected so that the output 62 of the electrical-potential-difference error amplifier 59 may be undergone, and Y is connected to the output side of the current detection resistor 75. Moreover, an adder circuit 78 has the fixed gain k, and has the gain stage 80 connected between the output of the electrical-potential-difference error amplifier 59, and its X input. Gain k must be more sharply [than a unit, 0.01 / for example, /,] small, when it is expected that output voltage Vout and the criteria resistance Vref are almost equal. The output of a comparator 76 is connected to the monostable multivibrator 82, and the output is supplied to the drive circuit 83 through the logic inverter 84. The drive circuit 83 drives the switches 72 and 74 of a power circuit 68 including the high order driver 86 and the low order driver 88, respectively.
[0052] The actuation of the switching regulator circuit of drawing 9 is as follows. When the product of the current in Inductor L and the resistance RS of a resistor 75 exceeds the error voltage which the electrical-potential-difference error amplifier 59 generates, the output of the electrical-potential-difference comparator 76 serves as quantity, and carries out the trigger of the monostable multivibrator. The logic inverter 84 reverses the high power of a multivibrator 82,

makes the high order switch 72 changed to the high order driver 86 off, and makes ON change the low order switch 74 to the low order driver 88. Consequently, the current of Inductor L begins to decrease. After it has related timing interval Toff and timing interval Toff passes, a monostable multivibrator 82 reverses the condition of switches 72 and 74, and the current in Inductor L begins to increase it. An inductor current's excess of SURESHIHORUDO of a comparator 76 repeats a cycle. In order to perform output voltage adjustment, SURESHIHORUDO of the electrical-potential-difference comparator 82 is changed by the adder circuit 78 using the error voltage from the error amplifier 59.

[0053] If constituted according to this invention, the switching voltage regulator of drawing 9 will obtain the almost optimal load transient response shown in the simulation plot of the load current Iload and output voltage Vout as shown in drawing 10 a and drawing 10 b, respectively. In this example, the load current changes from 0.56A to 14.56A, and return (deltaIload=14A) and permission output voltage deflection deltaVout is 0.07V. The parameter value of a switching regulator is as follows.

[0054] Vin=5V, Vref=2.8V, L= 3 microhenries, C=10mF, Re=5mohm, RS=5mohm, k= 0.01, deltaIload=14A, deltaVout=0.07V.

[0055] Re of an output capacitor is admission within the limits defined by Re(max) =delta Vout/delta Iload, and comments on it being equal to 0.07V/14A=5mohm here.

[0056] In this example, since Vout (=Vref) is larger than Vin=Vout, m is given by the following formulas.

[0057]

[Equation 18] m=(Vin-Vout)/L=[(5-2.8) V] / 3 microhenry=0.733 A/mu s expression 1 to the critical capacity Ccrit is [0058] given by the following formula.

[Equation 19] Since Ccrit=14A/[(0.733A/mus) (5mohm)]=3.818mF10mF is larger than 3.814mF(s), as for C, R0 (given by the formula 5) becomes equal to Re more greatly than Ccrit therefore. In order to attain this, the electrical-potential-difference error amplifier 59 is compensated if needed, and the transfer function of a formula 4 is obtained. This compensation will be performed, if the following two formulas are satisfied when realizing the electrical-potential-difference error amplifier 59, as shown in drawing 9 .

[0059]

[Equation 20]

K*(R2/R1) =1/(g*R0) (formula 7)

[0060]

[Equation 21]

Re*C=R2*C1 (formula 8)

The value of g is determined by the transformer resistance of a current sensor 64, and the embodiment of the current controller 66. When the 1st step of a current controller is an electrical-potential-difference comparator (it is this case like), g is equal to the reverse of the transformer resistance of a current sensor 64. When realizing a current sensor by resistance, transformer resistance only serves as resistance of a resistor (therefore this example g= 1-/RS). When the following component values are used, it is satisfied with this example of a formula 7 and a formula 8.

[0061]

As the wave of R1=1kohm and R2=100kohm and 1= 500pF [of C] drawing 10 b shows, an output voltage response corresponds to the resistance output impedance of 5mohm, and is equal also to ESR of an output capacitor.

[0062] The 1 alternative embodiment of a feedback circuit 58 is shown in drawing 11 . Here, the electrical-potential-difference error amplifier 59 is realized using the transconductance amplifier 90. Transconductance amplifier is characterized by the output current being proportional to the electrical-potential-difference difference between a noninverting input and a reversal input. The proportionality coefficient between the output current and an input difference electrical potential difference serves as the transconductance gm of amplifier. The voltage gain of transconductance mold electrical-potential-difference error amplifier is equal to the product of the impedance connected to the output of the transconductance amplifier 90, and Transconductance gm.

[0063] The embodiment of the electrical-potential-difference error amplifier shown in drawing 9 and drawing 11 serves as equivalence, when satisfying the following three formulas.
[0064]
[Equation 22]
gm[(R3R4)/(R3+R4)] =R2/R1 Formula 9 [0065]
[Equation 23]
VCC[(R4)/(R3+R4)] =Vref Formula 10 [0066]
[Equation 24]
C2 [[(R3R4)] / [/] (R3+R4)] =C one R2 Satisfaction of each of a formula 11 therefore a formula 9, a formula 10, and a formula 11 obtains the transfer function defined as the formula 4 about the electrical-potential-difference error amplifier 59 shown in drawing 11 .
[0067] This invention is not necessarily limited to using with the current modal-control mold voltage regulator containing electrical-potential-difference error amplifier. One possible operation gestalt of this invention which does not use current modal-control or electrical-potential-difference error amplifier, either is shown in drawing 12 . With this operation gestalt, the good control power stage 100 generates output voltage Vout according to the electrical-potential-difference difference between one pair of inputs 102, and 104. A power stage includes the power circuit 68 controlled by the high-speed electrical-potential-difference controller 105 which receives an input. In a switching voltage regulator, the high-speed electrical-potential-difference controller 105 has the description of enlarging quickly the duty ratio of the pulse train in the output, when the forward electrical-potential-difference difference which may be perceived appears between an input 102 and 104. In a linearity voltage regulator, the high-speed electrical-potential-difference controller 105 is usually realized using a broadband operational amplifier.
[0068] Moreover, the operation gestalt of drawing 12 generates the output changed with the output current of a regulator also including the current sensor 106 which has the transformer resistance RS connected to the serial between the output of the power stage 100, and the output node 52. The output of a current sensor is connected to one input of an adder circuit 108, and the 2nd input of an adder circuit is connected to the output node 52. An adder circuit generates output voltage equal to the sum of the input, and connects it to the input 102 of the power stage 100.
[0069] The input 104 of the power stage 100 is connected to the node 110 located in the join between one pair of impedances Z1, and Z2. Impedances Z1 and Z2 are connected to the serial between the output node 52 and the electrical-potential-difference criteria 112. As shown in drawing 12 , when it constitutes a regulator, an optimum transient response is obtained by adjusting the ratios Z2/Z1 of two impedances according to the following formula.
[0070]

[Equation 25]
Z2 / Z1=[(R0(1+sReC)-RS] /RS (formula 12))
Here, R0 is defined by the formula 5 and the formula 6, RS is resistance of a current sensor 106 and Re and C are ESR and capacity of the output capacitor 56 to adopt.
[0071] One embodiment of the operation gestalt of the voltage regulator of drawing 12 is shown in drawing 13 . The high-speed electrical-potential-difference controller 105 is realized by the hysterics tele tick comparator (hysteretic comparator) 130, and the output is connected to the drive circuit 132. The drive circuit 132 contains the high order driver 134 and the low order driver 136. A power circuit 68 is driven by drivers 134 and 136 including the high order switch 138 and the low order switch 140, respectively. The output inductor L is connected to the joint during a switch. The hysterics tele tick comparator 130 turns OFF a high order switch, when output voltage is supervised and output voltage exceeds top SURESHIHORUDO of a comparator. A high order switch is again turned on, when output voltage falls under to bottom SURESHIHORUDO of a comparator.
[0072] The current sensor 106 and the adder circuit 108 are realized by the series resistance machine 142 which has Resistor RS. An impedance Z1 is realized by the parallel connection of a capacitor C4 and a resistor R6, and the impedance Z2 is realized by resistance R7.
[0073] In order for the output impedance of the switching regulator of drawing 13 to become equal to resistance R0, the resistance ratio of resistors R6 and R7 must be given by the following formula.
[0074]
[Equation 26] R7 / R6= (R0-RS) / RS and also the capacity of a capacitor C4, and the product of resistance of a resistor R6 must be given by the following formula.
[0075]
[Equation 27] C4R6=C[(R0Re)/R3]
Although it will accept to this contractor in the engineering of a voltage regulator easily, the embodiment and operation gestalt of a voltage regulator which were discussed previously are only only instantiation. As long as it carries out so that the approach of this invention may be indicated here even if it uses much of other circuitry, the optimal transient response and the target of this invention called the output capacitor minimum as much as possible can be attained.
[0076] The approach of this invention indicated here can be shown as a general design procedure, can be applied to the design of both linearity and a switching voltage regulator, and corresponds also to use of both output capacitor that has the output capacitor and the capacity below this which have the capacity exceeding the critical capacity defined previously. This design procedure can be carried out according to the following steps.
[0077] 1. Choose the class of classes (aluminum electrolyte, a ceramic, OS-CON capacitor, etc.) of capacitor used as an output capacitor of a voltage regulator required in order to maintain regulation output voltage within voltage deviation specification deltaVout specified to step change deltaIload in the load current.
[0078] 2. Determine the property time constant TC to the class of selected capacitor. This is defined as a product of the ESR and its capacity, as explained previously.
[0079] 3. Determine the absolute value of the inclination for minimum good of the current poured in towards the parallel connection of an output load and an output capacitor to step-like increase of the load current equal to deltaIload to step-like reduction of the load current equal to the absolute value and deltaIload of the inclination for maximum good of the current which a

voltage regulator pours in towards the parallel connection of an output load and an output capacitor. This is performed as the formula 1 was explained.
[0080] The smaller one is determined among 4.2 absolute values. The absolute value of the smaller one is identified as m.
[0081] 5. Determine the 1st capacity C0 according to the following formulas.
[0082]
[Equation 28]
Resistance Re 0 is determined according to the formula below C0=[deltaIload2 / 2 m+mTC2/2]/deltaVout6.
[0083]
[Equation 29] The critical capacity value Ccrit is determined according to the formula below Re0=TC/C07.
[0084]
[Equation 30] In Ccrit=delta Iload/mRe08.C0<Ccrit, the output capacitor which has the equivalent series resistance Re 1 almost equal to the capacity C1 and Re0 almost equal to C0 is used.
[0085] In C0 >=Ccrit, the output capacitor which has the equivalent series resistance Re 2 almost equal to delta Vout/delta Iload and the capacity C2 almost equal to TC/Re0 is used.
[0086] 9. Determine resistance R0 according to the following formulas. In C0<Ccrit, it is [0087].
[Equation 31] In R0=deltaIload/2mC1+[mC1 (Re1)] / 2deltaIloadC0 >=Ccrit, it is [0088].
[Equation 32] A voltage regulator is adjusted so that the output impedance of a voltage regulator defined before connection with the output capacitor of which R0=Re210. use is done may become almost equal to the series connection of resistance R0 and an inductance L0. L0 is given by the following formula.
[0089] In C0<Ccrit, it is [0090].
[Equation 33] In L0=C1*Re1*R0C0 >=Ccrit, it is [0091].
[Equation 34] L0=C2*Re2*R0 -- this step is performed by making the transfer function of the feedback circuit of a regulator correspond to a formula 4 according to the above-mentioned approach.
[0092] It comments on a time constant TC (or the configuration coefficient C and Re) not being the amount correctly defined to each capacitor kind. All of the factor of a large number containing a manufacture allowable error, case size, temperature, and a voltage rating can affect TC. Therefore, in an actual design, it may be required to regard the parameter TC used for count as approximate value, and to repeat a design procedure a certain number of times.
[0093] Moreover, especially the approach of this invention can be shown as a procedure for the design of the back mold switching voltage regulator which adopts current modal control. This guarantees maintaining the output voltage Vout within voltage deviation specification deltaVout specified to step change deltaIload of the load current, holding down the size of the output capacitor of a regulator to min. This kind of regulator has one pair of switches connected to the serial between input voltage Vin and touch-down, and the joint during a switch is connected to the output inductor. A switch is driven so that an inductor may be connected to Vin and touch-down by turns. Only in C>Ccrit, the following design procedures can be applied and it comments on the optimal load transient response shown in drawing 6 a in that case being obtained. Moreover, by following the above-mentioned design procedure, it is possible to use the output capacitor which has the capacity of under Ccrit, and the back mold regulator which adopts

current modal control can also attain the optimum response shown in drawing 7 a by this. A design procedure applicable in C>Ccrit can be carried out by the following steps.
[0094] 1. Calculate the maximum equivalent series resistance Re (max) to the output capacitor of a regulator according to the following formulas.
[0095]
[Equation 35] According to the formula below Re(max) =delta Vout/delta Iload2., the minimum inductance Lmin to the output inductor of a regulator is determined.
[0096]
[Equation 36]
Lmin=(VoutToffRe (max))/Vripple and p-p -- here, the off time amount of the switch whose Toff connects an output inductor to Vin, Vripple, and p-p are maximum-permissible peak pair peaking capacity ripple voltages.
[0097] 3. Use the output inductor which has the inductance L1 more than Lmin.
4. Determine the minimum capacity Cmin of an output capacitor according to the following formulas.
[0098]
[Equation 37] Vout -- < (Vin-Vout) -- a case -- Cmin=deltaIload/[Re (max) (Vout/L1)]
[0099]
[Equation 38] In Vout>Vin-Vout, it is Cmin=deltaIload/[Re(max) ((Vin-Vout) / L1)].
5. Use the equivalent series resistance Re almost equal to the output capacitor which has the capacity C almost equal to Cmin, and Re (max).
[0100] 6. Constitute the output impedance of a regulator so that it may become almost equal to Re. This step is performed according to the above-mentioned approach by making the transfer function of the feedback circuit of a regulator matched with a formula 4.
[0101] The specific operation gestalt of this invention is shown above, and although explained, deformation of a large number and an alternative implementation gestalt will also be recollected by this contractor. For example, there are some which permuted the 2nd switch by one of the alternative implementation gestalten in which the back mold switching regulator was common with rectifier diode. Therefore, it shall mean that this invention is restricted only about the attached claim.

CLAIMS

[Claim(s)]
[Claim 1] Maintain the output voltage of a regulator within the boundary specified to the bidirectional step change in the load current. It is the approach of making it possible to a voltage regulator to use the minimum output capacitor as much as possible. A voltage regulator with required within the boundary which adopted the output capacitor (56) and was specified to the bidirectional step change in the load current maintaining regulation output voltage (Vout) It consists of the step compensated so that the response may become flat after the output voltage reaches the peak deflection. The approach that said output capacitor required in order to perform said compensation is characterized by the thing which maintains the output voltage of said regulator within said specified boundary and which it is said output capacitor minimum as much as possible.

[Claim 2] Maintain the output voltage of a voltage regulator within voltage deviation specification deltaVout specified to bidirectional step change deltaIload in the load current. It is the approach of minimizing the size of the output capacitor of said regulator. It is the step which calculates the maximum equivalent series resistance Re (max) of the output capacitor (56) which the voltage regulator which supplies output voltage (deltaVout) to a load (RL) in an output node (52) adopts. Said output capacitor is connected to juxtaposition between said loads. Said regulator It is necessary to maintain the output voltage of a voltage regulator within voltage deviation specification deltaVout specified to bidirectional step change deltaIload in the load current. The step which calculates Re (max) according to Re(max) =delta Vout/delta Iload, It turns to the parallel connection of said output load and an output capacitor to the increment in a step in the load current equal to deltaIload. As opposed to the step reduction in the load current equal to the absolute value and deltaIload of the inclination for maximum good of the current which said voltage regulator pours in The step which determines the absolute value of the inclination for minimum good of the current poured in towards the parallel connection of said output load and an output capacitor, The step which judges the smaller one among said absolute values, and makes a value m the one where this absolute value is smaller, The step which determines the critical capacity Ccrit according to Ccrit=delta Iload/mRe (max), The step chosen in order to connect the output capacitor which is somewhat smaller than Re (max), or has the capacity more than the equivalent series resistance Re and Ccrit equal to this between said loads, the step which constitutes the output impedance of said voltage regulator so that it may become almost equal to Re -- since -- the approach characterized by changing.

[Claim 3] The good control power stage to which said voltage regulator answers the signal received in a control input (53), and supplies the output voltage of said regulator in an approach according to claim 2 (50), The electrical-potential-difference error amplifier (59) connected between said output node and said control input is included. In case the step adjusted so that said power stage may become almost equal to Re about a characterization eclipse and said output impedance by Transconductance g is performed, it is [Equation 1] about gain [of said electrical-potential-difference error amplifier] K (s).

$$K(s)=(-1/gRe)(1/(1+sReC))$$

It is the approach which is alike, makes it equal and is characterized by what C and Re are said capacity and equivalent series resistance of an output capacitor which were adopted here.

[Claim 4] Make it possible to maintain the output voltage Vout of a back mold switching voltage regulator within voltage deviation specification deltaVout specified to bidirectional step change deltaIload in the load current. It is the approach of minimizing the size of the output capacitor of said regulator. Input voltage Vin Reception, It is the step which calculates the maximum equivalent series resistance Re (max) of the output capacitor (56) which the current control mold switching voltage regulator which supplies output voltage (deltaVout) adopts as the load (RL) connected to the output node (52) through the output inductor (L). Said inductor is connected to Vin and touch-down by turns with the 1st and 2nd switches (72 74). It connects with juxtaposition between said loads, said output capacitor needs to maintain Vout within voltage deviation specification deltaVout specified to bidirectional step change deltaIload [in / in said regulator / the load current], and it is [Equation 2] about Re (max). The step calculated according to Re(max) =delta Vout/delta Iload, and [Equation 3] the step which is a step which determines the minimum inductance Lmin to said output inductor according to Lmin=VoutToffRe(max)/Vripple and p-p, and chooses the step whose Toff is a maximum-permissible peak pair peaking capacity ripple voltage here for the off time amount of said 1st

switch, Vripple, and p-p, and the output inductor in which it has the inductance L1 more than Lmin in order to use it in said regulator, and Vout -- < (Vin-Vout) -- a case -- [Equation 4]
Cmin=deltaIload/[Re (max) (Vout/L1)]
It is [Equation 5], when it is alike, it follows and it is Vout>Vin-Vout.
Cmin=deltaIload/[Re(max) ((Vin-Vout) / L1)]
the step which chooses in order to connect the output capacitor which has the step which is alike, follows and determines the minimum capacity Cmin of said output capacitor, and the capacity C almost equal to Cmin, and the output capacitor which has the equivalent series resistance Re almost equal to Re (max) between said loads, and the step which constitute the output impedance of said regulator so that it may become almost equal to Re -- since -- the approach characterized by to change.
[Claim 5] It is the voltage regulator which maintains output voltage within voltage deviation specification deltaVout specified to bidirectional step change deltaIload in the load current. It connects so that output voltage Vout may be generated to an output node (52) according to the signal received in a characterization eclipse and a control input (53) by Transconductance g. The good control power stage where said output node is connected to the load (RL) (50), The output capacitor which is an output capacitor (56) which was connected to said output node and connected to juxtaposition between said loads, and has equivalent series resistance Re, It has the electrical-potential-difference error amplifier (59) connected between said output nodes and said control inputs. Said good control power stage, said output capacitor, and said amplifier within voltage deviation specification deltaVout specified to step change deltaIload in the load current The voltage regulator which needs to maintain the electrical potential difference in said output node is formed, said output capacitor has the capacity more than the critical capacity Ccrit, and it is [Equation 6] about this critical capacity Ccrit. It determines according to Ccrit=delta Iload/mRe. Here m 1) As opposed to the increment in a step in the load current equal to deltaIload As opposed to the step reduction in the load current equal to the absolute value and 2Iload of the inclination for maximum good of the current which said voltage regulator pours in towards the parallel connection of said output load and an output capacitor Are equal to the smaller one among the absolute values of the inclination for minimum good of the current which said voltage regulator pours in towards the parallel connection of said output load and an output capacitor. The voltage regulator characterized by what is constituted so that said voltage regulator may have an output impedance almost equal to Re.
[Claim 6] It sets to a voltage regulator according to claim 5, and gain [of said electrical-potential-difference error amplifier] K (s) is [Equation 7].
K(s)=(-1/gR0)(1/1+sReC))
It is the approach that be alike is given, g is equal to the transconductance of said good control power stage here, and Re and C are characterized by the thing respectively equal to the equivalent series resistance and capacity of said output capacitor.

[Claim 7] Said capacitor is a voltage regulator to which it is characterized by being the output capacitor minimum as much as possible which makes it possible to maintain the output voltage within deltaVout to step change deltaIload [in / in a voltage regulator according to claim 5, it has the equivalent series resistance Re with said output capacitor almost equal to a capacity almost equal to Ccrit, and delta Vout/delta Iload, and / in a voltage regulator / the load current].
[Claim 8] It is the voltage regulator which maintains regulation output voltage within voltage deviation specification deltaVout specified to step change deltaIload in the load current. The

good control power stage which supplies output voltage (Vout) to a load (RL) in an output node (52) according to the electrical-potential-difference difference between the 1st control input (102) and the 2nd control input (104) (100), Said output node and the output capacitor connected to juxtaposition between said loads (56), The impedance Z1 connected between said output node and the 1st node (110), The impedance Z2 connected between said 1st node and reference voltage (Vref), The current sensor which generates the output voltage (Vout) changed with the output current (Iout) which has the transformer resistance RS and is sent out to said load (106), It has the adder circuit (108) which generates output voltage equal to the sum of said sensor output voltage and the electrical potential difference in said output node. Said current sensor output voltage and said adder-circuit output voltage, respectively It connects with said 1st and 2nd control inputs. Said good control power stage, said output capacitor, Within voltage deviation specification deltaVout as which said impedance, said current sensor, and said adder circuit were specified to step change deltaIload in the load current The voltage regulator which needs to maintain the electrical potential difference in said output node is formed, and, for said regulator, the ratio of impedances Z1 and Z2 is [Equation 8].

Z1 / Z2=[(R0(1+sReC)-RS] it is constituted so that it may become equal to /RS here, Re and C) Respectively, it is equal to the equivalent series resistance and capacity of said output capacitor, and R0 is equal to Re, when C is more than deltaIload/mRe. When C is under deltaIload/mRe, are equal to deltaIload / 2mC+[mC (R<SUB>e)] / 2deltaIload. Or m 1) As opposed to the increment in a step in the load current equal to deltaIload As opposed to the step reduction in the load current equal to the absolute value and 2deltaIload of the inclination for maximum good of the current which said voltage regulator pours in towards the parallel connection of said output load and an output capacitor The voltage regulator characterized by the thing equal to the smaller one towards the parallel connection of said output load and an output capacitor among the absolute values of the inclination for minimum good of the current which said voltage regulator pours in.

[Claim 9] Said impedance Z1 is realized in a voltage regulator according to claim 8 by the resistor R1 and capacitor C1 which were connected to juxtaposition, an impedance Z2 is realized by resistance R2, said resistance R1 and R2 and capacitor C1 are constituted so that the output impedance of said voltage regulator may become equal to Re, and it is [Equation 9] by this. R2 / R1= (R0-RS) / RS, and [Equation 10] C1*R1=C[(R0Re)/RS]

The voltage regulator which comes out and is characterized by a certain thing.

[Claim 10] The voltage regulator which said current sensor and adder circuit are equipped with the resistor which has the resistance RS connected between said good control output stage in the 2nd node, and said output node in a voltage regulator according to claim 8, and is characterized by the electrical potential difference in said 2nd node being the output voltage of said adder circuit.